Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER B.Tech. DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: BASIC ELECTRONICS (ECE - 1001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the self-bias circuit using BJT. Explain how bias stability is achieved in this circuit. For a self-bias circuit if I_C=1mA, V_{CC}=12V, $V_{CE}=V_{CC}/2$, $V_B=V_{CC}/10$, β =100, V_{BE}=0.6V, R_2=2kΩ, Determine R_1, R_C & R_E.

1B. Explain the static & dynamic resistances of diode. Calculate the static & dynamic resistances of a silicon diode for forward and reverse applied voltage of 0.25 V. Given I_0 = lμA and T = 300^0 K.

1C. Using operational amplifiers realize the equation V_o= - ($0.1V_a$ +V_b+$10V_c$) where, V_a, V_b, V_c are inputs.

(5+3+2)

2A. Draw neat circuit diagram of bridge rectifier using diodes and explain the functioning. Illustrate with relevant waveforms. Obtain expression for V_{dc} and ripple factor. Describe how the ripples at the dc output can be reduced.

2B. Write the truth table of full adder circuit. Obtain expressions for the sum & carry outputs and implement using two half adder logic circuits.

2C. Subtract $(73.625)_{10}$ from $(111.26)_8$ using 2's complement method.

(5+3+2)

3A. Simplify the following Boolean expression f(a,b,c,d)=∑m(0,2,3,4,5,7,8,10,11,12,13,14,15) using K-Map and implement using only NAND gates.

3B. Realize a 3-bit down counter using negative edge triggered JK flip flops. Draw the timing diagram for the same.

3C. Bring out the difference between Latch and Flip-flop. Draw the logic circuit of a JK flip-flop using only NAND gates.

(5+3+2)

4A. Differentiate between sequential & combinational circuits. Serial input data 11100110 is fed to the 4-bit shift register circuit from LSB. What will be the output for SISO operation after 6^{th} clock pulse? How many clock pulses are required to shift MSB bit to the output. Also draw the circuit diagram.

4B. Draw the block diagram of digital communication system and highlight the function of each block.

4C. Draw the ASK and FSK signals for the binary information 10010.

(5+3+2)

5A. Define amplitude modulation. Sketch the spectrum of AM signal indicating sideband frequencies, amplitudes and bandwidth. A certain AM transmitter radiates 9 kW of power with carrier unmodulated and 10.125kW of power when carrier is sinusoidally modulated. Calculate the modulation index.

5B. With reference to sinusoidal modulating signal, draw the typical waveforms of PAM, PPM and PWM signals.

5C. Consider a FM signal, V_{FM} (t) = 10 cos [$2\pi 10^8$t +5 $sin(2\pi\ 15000t)$]. Calculate its frequency sensitivity and bandwidth using Carson's rule.

(5+3+2)