Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent institution of MAHE, Manipal)

IV SEMESTER B.TECH. (BME) DEGREE MAKEUP EXAMINATIONS JUNE 2018

SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Thursday, 21st June 2018: 2 to 5 PM

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. **Answer ALL the questions.**
2. **Draw labeled diagram wherever necessary**

1. (a) What is a "Semicustom IC" and explain. Give an example. 05

   (b) What is *top down* design approach? Explain. 07

   (c) Design a CMOS inverter gate. Explain the circuit operation. Compare it with a simple nMOS inverter circuit. 08

2. (a) Draw the neat diagram of SRAM cell and explain. 06

   (b) What are Programmable Logic devices? Draw the architecture of a simple PLD and explain. 06

   (c) Draw the programmed state of an AND-OR plane of a Programmable Logic Array (PLA) for the following: $f = x_1\bar{x}_2 + \bar{x}_1 x_2$. 08

3. (a) What is transmission gate (TG)? Design a noninverting buffered 2:1 multiplexer using TG and inverters. Explain its operation. 10

   (b) Use Shannon's expansion theorem in the following cases to implement the function: $f = \bar{w}_1\,\bar{w}_3 + w_1 w_2 + w_1 w_3$: 10

   i) Design the circuit using 2 to 1 MUX and any other necessary gates, using w_1

   ii) Design the 4 to 1 MUX and any other necessary gates, using w_1 and w_2

4. (a) What is FPGA? Draw the diagram of a CLB (Configurable Logic block) of a FPGA and explain. 10

(b) Write a Verilog module for design a 2 to 1 MUX. 05

(c) What are non-blocking statements? Explain its significance in the design of a sequential circuit 05

5. (a) What are benefits of Programmable Array Logic (PAL) over Programmable Logic Array(PLA). With a neat diagram explain the elements of a PAL. 10

(b) Write a Verilog HDL module for realizing a Full adder. 05

(c) Describe "behavioral style" of designing a digital system design using Verilog HDL module. 05