Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent institution of MAHE, Manipal)

IV SEM B.TECH. (BME) DEGREE END SEMESTER EXAMINATIONS APRIL 2018

SUBJECT: DIGITAL SYSTEM DESIGN (BME 2203)
(REVISED CREDIT SYSTEM)
Wednesday, 25th April 2018, 2 to 5 PM

TIME: 3 HOURS **MAX. MARKS: 100**

Instructions to Candidates:

1. **Answer ALL the questions.**
2. **Draw labeled diagram wherever necessary**

1. (a) How is an Application Specific Integrated Circuit (ASIC) different from a standard IC?. Explain the *Semi-customized Application Specific Integrated Circuit*. 06

   (b) Explain the design flow of an ASIC. 06

   (c) Design a two input CMOS NOR gate. Verify the truth table associated with the circuit, considering ON/OFF state of the transistor. 08

2. (a) Draw the architecture of a typical Complex Programmable Logic Device (CPLD), and explain its functioning. 06

   (b) Draw the diagram of transmission gate based latch and explain its operation. 06

   (c) Realise the given function: $f(w1, w2, w3) = \sum m(2,3,6)$ using nMOS based PLA. Draw the programmed state of the AND-OR plane with all the details labelled. 08

3. (a) State *Shannon's* expansion theorem that helps in the realization of a logic function using a 4 to 1 multiplexer. 04

   (b) Expand the logic function "*f*" given in Q 2 (c) using *Shannon's* expansion theorem, and realize the function in terms of a 4 to 1 multiplexer. Draw a labelled diagram with all variables. 06

(c) Design a two input LUT for implementing the following function: 04

$f = x_1 \overline{x_2} + x_1 x_2$

(d) Design a *4-bit array multiplier* using the following logic blocks: full adder/Half adder and basic gates. 06

4. (a) Describe the significant difference between the architecture of channeled and channel-less Gate-Array-based ASICs. 06

(b) Draw the generalized architecture of PAL, along with its extended logic cell. Explain the major elements of the *macrocell a*nd its significance. 08

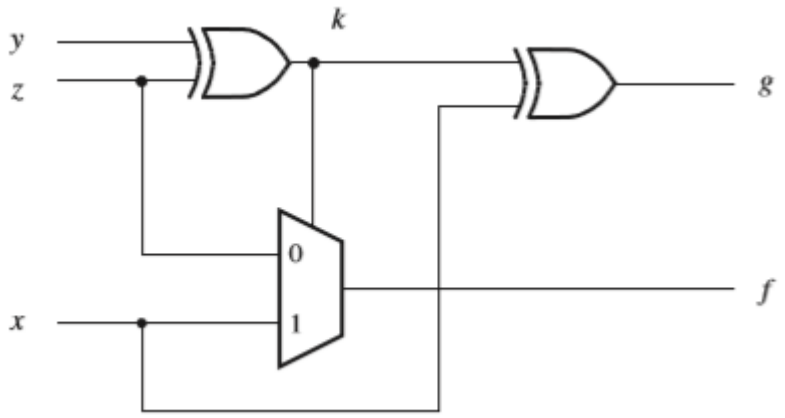
(c) Design a Verilog module of a decoder with the following specifications:

- Output put: Active low vectored notation
- Design style: dataflow type
- Time unit: 1ns/100ps.

06

5. (a) Draw the architecture of a FPGA. Explain the details of CLB (Configurable Logic block) and the switching technology used in the switch matrix of FPGA. 08

(b) Write a Verilog HDL module for the digital circuit given in figure 5(b).



05

Fig. 5 (b)

(c) Design a Verilog HDL module of the *4-bit shift* Register using the concept of module instantiation. Use *connection by name* syntax for creating instance. Draw the associated hardware details. 07