Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B. Tech. (E & C) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: I C SYSTEMS (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. For the circuit in Fig. Q.1A, determine the value of A_c, A_d and CMRR. Assume identical transistors with β=100, supply voltage ± 10V and V_{BE} of 0.7V. Modify this circuit and design to achieve very high CMRR maintaining same value of biasing current in the differential amplifier.

1B. Following measurements were made for an Op-Amp when the input voltage is connected between the two input terminals: (i) Output is 2V when the load resistance $R_L=\infty$, and (ii) Output is 1.8V when the load resistance $R_L=675\Omega$. (a) Find the output resistance of an Op-Amp. (b)What must be the ideal value of output resistance and why?

1C. The biasing voltage at the output of second stage (DIUBO) of an Op-Amp is 6V. The current mirror circuit is used to supply current of 4.22mA to all stages of an Op-Amp. Design the level shifter so as to shift the biasing dc voltage to zero. Assume V_{BE} of 0.7V.

(5+3+2)

2A. Draw the input/output voltage waveforms of an Op-Amp which has Gain of 100dB, Slew rate 0.5V/µsec in each of the following cases: Assume supply voltage ± 10V and zero output offset voltage.

(i) $V_{inverting} = 10\ Sin(314t)$ µV and $V_{non-inverting} = 40\,Sin(314t)$ µV

(ii) $V_{inverting} = 500\,Sin(314t)$ µV and $V_{non-inverting} = 50\ Sin(314t)$ µV

(iii) $V_{inverting} = 10\ Sin(3140000t)$ µV and $V_{non-inverting} = 0$ V.

(iv) $V_{inverting} = 0$ V & $V_{non-inverting}$ = Square wave: 1 V for 20µsec and -1 V for 80 µsec.

2B. Design a circuit to implement $Vo = \frac{d^2 Vi}{dt^2}$. Assume input signal has a maximum frequency of 2 kHz

2C. With the help of the circuit diagram and waveforms, explain the working of Peak detector.

(5+3+2)

3A. Design a square wave generator using Op-amp, for the following specifications:
Frequency of oscillation = 1 kHz, duty cycle = 30 % , peak to peak output voltage = 12.4V ,
Assume capacitance of 0.01µF, V_{sat} = ± 10V, β = 0.5 .

3B. Plot the frequency response of the filter shown in Fig.Q3B.

3C. Derive the expression for the phase shift provided by the phase corrector for the input signal.

(5+3+2)

4A. Design a Butterworth filter having a frequency response as shown in Fig. Q4A. Select C = 100nF

4B. Using 555 timer, design a circuit which produces the wave form shown in Fig Q4B.

4C. Draw the internal diagram of 555 timer and name all the pins.

(5+3+2)

5A. Draw the circuit diagram of a 4-bit binary weighted resistor type DAC and derive the expression for the output voltage. Determine the output when the input is 1010. What is the resolution of the DAC. Select R = 10kΩ, V_{FS} = -10 V, Logic 0 = 0 V and Logic 1 = 5V.

5B. Using PLL, design a circuit to get 10kHz clock frequency from 1kHz clock frequency and explain its working.

5C. Derive the 8-bit digital output equivalent of an analog voltage of 6V for an 8-bit dual slope ADC, which has a maximum integrator output of -8V when the input voltage is 12V.

(5+3+2)

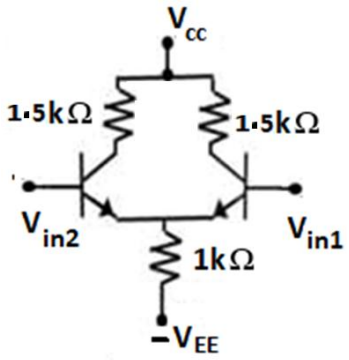

Fig. Q1A

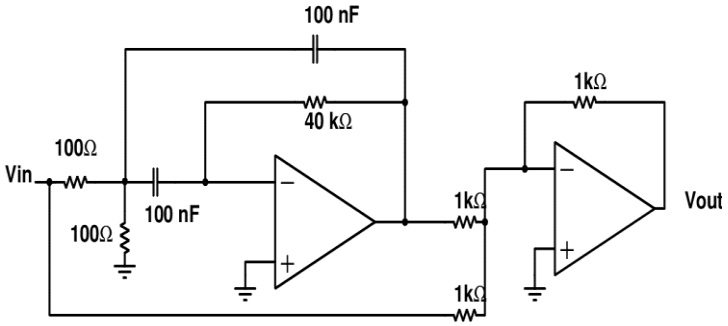

Fig. Q3B

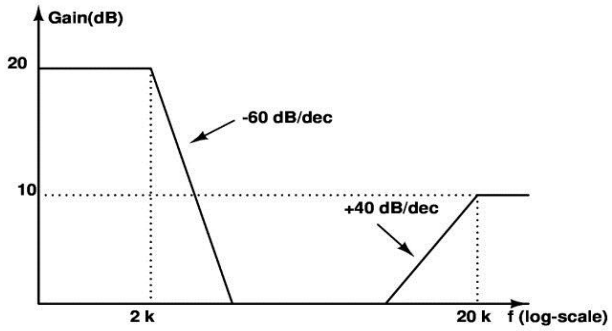

Fig Q4A

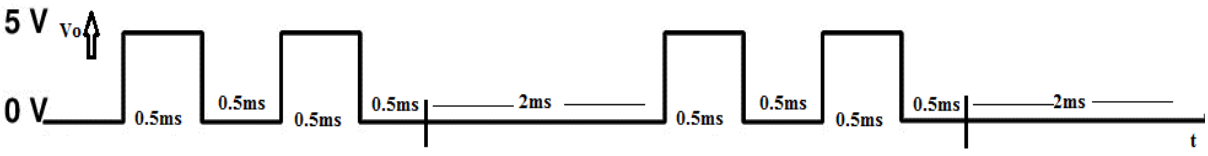

Fig Q4B