Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH. COMPUTER SCIENCE AND ENGINEERING

END SEMESTER EXAMINATIONS, APRIL 2018

SUBJECT: MICROPROCESSORS [CSE 2203]

REVISED CREDIT SYSTEM
25.04.2018

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL FIVE** questions.
- Missing data may be suitable assumed.

1A. State the two categories of flags in 8086 flag register. Write how you will set or reset the flags which falls into these two categories. Also list the two instructions that can adversely affect the pipelining process in 8086. **3M**

1B. Explain the following assembler directives with an example **3M**
i) EQU ii) DD iii) OFFSET

1C. Assume the contents of various 8086 registers in hexadecimal as follows. **4M**
DS: SI=1345:0018, DS: DI= 1345:00B1, DS:BX=1345:12A0 and CS=538A and the specified instructions are present at the given offset addresses. Perform the following for each of the instruction specified below in the table Q1C.

i) Write the addressing mode for the destination operand
ii) calculate the physical address in hexadecimal for the instruction
iii) Calculate the effective address and physical address in hexadecimal for the byte/word read or written to/from the memory.

Table Q1C

OFFSET	**INSTRUCTIONS**
001C	MOV [SI],CL
ABCD	SUB 15[BX+DI],CL

2A. State one advantage and disadvantage when using stack to pass parameters to the procedure. Also explain the two different forms of indirect jump with an example. Identify the type of jump instruction for the following if **4M**

i) The displacement is 600H bytes
ii) The displacement is 0DF bytes

2B. Write equivalent instruction sequences using string instructions for each of the following: **2M**

i) MOV AX,[SI]
INC SI
INC SI

ii) MOV AL,[DI]
CMP AL,[SI]
DEC SI
DEC DI

2C. Write a complete 8086 assembly language program to pass an array of bytes as parameter to the procedure. The procedure has to calculate the largest nibble in each element in the array and store the result in another output array. If both the nibbles of an array element is equal, replace that element with zero in the output array. Display the output array in the standard output device. Assume the array input in the memory as two digit hexadecimal numbers and pairwise nibbles of each element are numbers. **4M**

3A. With the aid of a neat block diagram, explain how a single 8259A is connected to an 8086 microprocessor. Also mention the purpose of STI instruction and EOI command in the Interrupt Service Procedure (ISP) of an Interrupt Request line in 8259A. **4M**

3B. What memory locations contain the vector for an INT 44H instruction? Also explain how 8086 responds when it has an interrupt related to overflow and also receiving an interrupt request through INTR pin at the same time? Assume INTR pin of 8086 is enabled. **3M**

3C. How is an 8255A configured if its control register contains 9Bh? Justify this statement simple strobe method in 8255A will not work for high rates of data transfer. What solution you will propose to rectify this disadvantage with simple strobe method? **3M**

4A. Identify and explain the pins for the following in 8086 **3M**
i) Exclusive for data transfer
ii) Hardware Interrupt

4B. Write how an 80286 is switched from real address mode to protected virtual address mode and how it is switched back to real address mode operation. Show the computations which tell how much physical memory and virtual memory an 80286 can address. **3M**

4C. List the two major additions to the memory system of 80486 as compared to that of 80386.Also discuss the following signal groups of 80486 **4M**
i) Parity
ii) Bus cycle definition

5A. With the aid of a neat diagram, discuss how 80386 computes a physical address when its paging mode is enabled. **4M**

5B. Suppose a double word data is to be stored at an address 00000050H in a Pentium processor, identify the bank enable signals that needs to be activated. Justify your answer. Also define hyper threading in Pentium4 and Core 2 processor. State the case in which a hyper threaded Pentium 4 processor runs slower when compared to a dual processor system. **2M**

5C Discuss the role of each functional part in the internal structure of Pentium Pro. **4M**