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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER MAKE UP EXAMINATIONS, JUNE 2018

SUBJECT: MICROPROCESSORS [CSE 2203]

REVISED CREDIT SYSTEM

(21/06/2018)

Time: 3 Hours

MAX. MARKS: 50

Instructions to Candidates:

- ❖ Answer **ALL** the questions.
- ❖ Missing data may be suitably assumed.

- 1A.** Perform the following with respect to each of the instructions given below:
- i) Identify and explain the addressing mode used for the destination.
 - ii) Compute the effective address and the physical address of the memory location referred. Assume DS = 5000H, ES = 6000H, SS = 7000H, AX = 4235H, CX = 0004H, SI = 4000H, BP = 2468H.
- a) MOV [BP+SI], AX
- b) ADD N, CL where N is the fifth word memory location in the data segment **4M**
- 1B.** Write an 8086 assembly language program to remove all duplicate characters except space from a sentence present in the memory. Store the result as a new string in the memory. Example: input = Manipal Institute, result = Mnipl Istue. **4M**
- 1C.** Explain the following 8086 assembler directives with an example for each
- i) LABEL
 - ii) EQU **2M**
- 2A.** In an 80386 system, suppose the root address of a page directory is D0000000H and the 3rd entry (starting from zero) in this page directory is 70000000H that is the base address of a page table. The 4th entry (starting from zero) in this page table is C0000000H then what is the physical address corresponding to the logical address 00C04FFFH? Write the steps of calculation. Use these data to explain the paged memory system and the computation of physical address in 80386 when its paging mode is enabled with a neat diagram. Show the entries in all the tables in the diagram. **5M**
- 2B.** List the limitations of passing parameters to a procedure in dedicated memory locations. Explain a method with a program example to overcome these limitations. **3M**
- 2C.** A printer is connected to 8086 system. When the data is ready to print microprocessor sends a signal to the printer indicating that it has some data to print. In response to this signal printer sends back a signal accepting the processor's request. Indicate the data transfer mechanism suitable for the above situation and explain it with necessary waveforms. **2M**

- 3A.** Classify the following instructions into minimum and maximum mode instructions of 8086 and explain them.
- i) $\overline{SS0}$ ii) $\overline{S2}, \overline{S1}, \text{ and } \overline{S0}$ iii) DT/\overline{R} iv) \overline{LOCK} **4M**
- 3B.** Write an 8086 assembly language program to accept a sentence and a single digit number from the user and to replace the n^{th} word in the reverse order. Assume that sentence starts with a character and the words in the sentence are separated by one or more spaces. Display the new sentence on the monitor screen. Example: input sentence: Apple a day keeps doctor away. Input number: 3. Output: Apple a yad keeps doctor away. **3M**
- 3C.** Consider a system consisting of one 8086 and two 8259s in the master slave environment. The slave is connected to IR7 of the master. The AEOI bit in the ICW4 for the master is set. Slave has fixed priority and normal EOI. All IRs in the master are unmasked and IR3 is unmasked in the slave. Suppose when master is servicing interrupt at its IR0, slave receives the interrupts at IR3 and IR5, explain the actions taken by the 8086, the master and the slave. **3M**
- 4A.** Compare the memory system in Pentium and Pentium pro microprocessors. Explain the role of Instruction fetch and Decode unit and Retire unit in Pentium pro. **4M**
- 4B.** Describe all the string instruction prefixes with an example for each **4M**
- 4C.** Compare hyper-threading to dual processing. **2M**
- 5A.** Describe the 80286 protected mode operation. Also explain the physical address calculation in this mode with a neat diagram. **5M**
- 5B.** Write a note on the following:
- i) Register set in Pentium 4 and Core2 processors
- ii) The memory system in Pentium II **3M**
- 5C.** How does Pentium handle simultaneous execution of instructions? **2M**