Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE UP EXAMINATIONS, JUNE 2018

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 21 June 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Explain the levels of abstraction of the Gajski's Y chart in detail. ***(04)***

1B. Develop an even parity generator and checker using gate level modeling for a 3 bit data input. ***(03)***

1C. Design a pulse waveform generator to generate the sequence

10111101011110101111 0…….. using Verilog HDL code. ***(03)***

2A. Develop a Verilog HDL code to detect the sequences 101 and 010 using mealy machine concept and to count the number of occurrence of the sequence ***(05)***

2B. Using D flip flop as the instance develop the structural model for a 4 bit left shift register. ***(05)***

3A. Using minimum number of instructions write a program that is equivalent to

$$X = \frac{A*B - C*D}{E*F}$$

i. Using two address instructions
ii. One address instructions
iii. Zero address instructions ***(03)***

3B. Perform 137/25 using Non Restoring division algorithm ***(04)***

3C. Explain the following addressing modes, with examples.

a) Absolute addressing mode

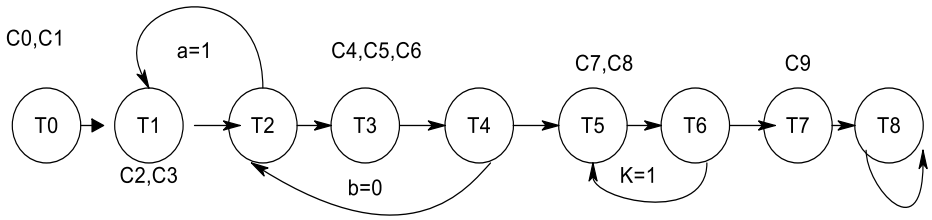
b) Immediate addressing mode

c) Register Indirect addressing mode ***(03)***

4A. For the below state diagram

a) Develop a Hardwired Control unit,

b) PLA design for the sequence controller



(05)

4B. A micro programmed control unit have 720 words by 80 bits, out of which 256 instructions are unique ,calculate the Microprogram code memory (MCM) and Nano Program code memory (NCM) and optimization achieved by saving number bits using Nano memory technology ***(02)***

4C. Explain the different types of interrupts and steps which involves when processor interrupted or INT pin activated on Processor Chip ***(03)***

5A. The Parameter of Computer Memory system are specified as follows:

Main memory size=8K

Cache memory size =512 blocks

Block Size =8 words

Determine the size of the tag field of the main memory address under the following conditions

a) Fully Associative Mapping

b) Direct Mapping

c) Set associative mapping with 16 blocks/set ***(02)***

5B. Write the difference between Paging and Segmentation ***(02)***

5C.

Starting address	block size
100	50
180	150
350	650
1100	400

Determine the available space list after allocating space for the stream of request consisting of the following block size 25,100,250,200

Use a) First fit method b) Best fit method ***(04)***

5D. With the neat diagram ,Explain FPGA Design flow ***(02)***