Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, APRIL 2018

SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 25 April 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Explain the IC fabrication steps in detail ***(04)***

1B. A lawn sprinkling system is controlled automatically by certain combinations of the following variables.

Season (S=1 , if summer ; 0 otherwise)

Moisture content of soil (M=1 , if high ; 0 if low)

Outside temperature (T=1 , if high ; 0 if low)

Outside humidity (H=1, if high ; 0, if low)

The sprinkler is turned on under any of the following conditions:

1. *The moisture content is low in winter*
2. *The temperature is high and the moisture content is low in summer*
3. *The temperature is high and the humidity is high in summer*
4. *The temperature is low and the moisture content is low in summer*
5. *The temperature is high and the humidity is low*

Write a gate level Verilog HDL code for turning ON the sprinkler system ***(03)***

1C. Using residual gates and 2 to 4 decoders develop a full subtractor and implement it using Verilog HDL code. ***(03)***

2A. Develop a behavioral Verilog HDL code for generating a 150Hz pulse from 10MHz clock pulse ***(02)***

2B. An Arithmetic Unit performs the following functions:

F	**Operation**
A + B	A plus B
A - B	A minus B
A +1	Increment A
A	Transfer A

where F is the output and A, B are the 1 bit inputs. Using a task for the 4 to 1 multiplexer and task for the full adder write the Verilog HDL code for the arithmetic unit

(05)

2C. Develop a counter to generate the sequence 8 – 4 – 2 – 1 – 8 – 4 – 2 – 1 - ……. Using Verilog HDL Display the output on the Seven Segment display ***(03)***

3A. Given an instruction set and the corresponding relative frequency, encode using Huffman's method and calculate the redundancy. Show how this is more efficient than Block code encoding technique.

Instruction	I0	I1	I2	I3	I4	I5	I6
Relative frequency count	0.05	0.1	0.4	0.18	0.2	0.04	0.03

(04)

3B. Perform **25 x -30** using Booth's algorithm ***(04)***

3C. Differentiate between RISC and CISC. ***(02)***

4A. Given below is the register transfer logic description of control unit. Develop the control signal, Draw the processing section and the state diagram.

Declare the registers: A[4], B[4], L[4], D[4], Q[4]

Start :A←0, D←0, B← In bus ;

Q←Inbus; /* Content of B, C, & Q are positive */

Loop1: D←B-C;

If D<>0 goto loop2;

A←A+1; Q←Q-1;

If Q<> 0 goto loop1;

Outbus ←D;

Loop2: Outbus ←A;

Halt; ***(05)***

4B. Determine the size of the Control Word when above Register transfer logic description implemented in Micro programming control unit and calculate the number of bits saved in each instruction using decoders ***(02)***

4C. Define and explain the following terms associated with pipeline processing

a) Speed up b) Efficiency c) Throughput ***(03)***

5A. With a neat diagram explain 4 level Hierarchical memory system and define the following terms

a) Average cost per bit b) Hit Ratio c) Average access time ***(03)***

5B. Assume that main memory has 3 pages frames and consider initially all the pages are empty. Consider following stream of references

2, 3, 2, 4, 6, 2, 5, 6, 1, 4, 6

Calculate the hit ratio if the replacement policy used is a) FIFO b) LRU ***(02)***

5C. Realise the following function using PLA ***(02)***

a) $F(a,b,c) = \pi M(1,3,4)$ b) F = X3X1+X2X1

5D. Explain the EPROM / EEPROM Program Technology used in ALTERA ***(03)***