Reg. No.



## MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent Institution of MAHE, Manipal)

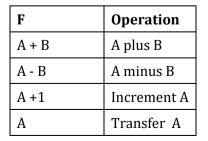
## **IV SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)**

## **END SEMESTER EXAMINATIONS, APRIL 2018**

## SUBJECT: DIGITAL SYSTEM DESIGN & COMPUTER ARCHITECTURE [ELE 2203]

**REVISED CREDIT SYSTEM** 

Time	e: 3 Hours	Date: 25 April 2018	Max. Marks: 50				
Instr	uctions to Candidates:						
	✤ Answer ALL the questions.						
	Missing data may be suitably	v assumed.					
1A.	Explain the IC fabrication steps in detail						
1B.	A lawn sprinkling system is controlled automatically by certain combinations of the following variables.						
	Season (S=1 , if summer ; 0 otherwise )						
	Moisture content of soil (M=1, if high ; 0 if low)						
	Outside temperature (T=1, if high; 0 if low)						
	Outside humidity (H=1, if high ; 0, if low)						
	The sprinkler is turned on under any of the following conditions:						
		,					
	1. The moisture content is low						
		nd the moisture content is low in summer					
		nd the humidity is high in summer d the moisture content is low in summer					
	5. The temperature is high a						
	r o	-	(03)				
	Write a gate level Verilog HDL code for turning ON the sprinkler system						
1C.	Using residual gates and 2 to 4 decoders develop a full subtractor and implement it using Verilog HDL code.						
2A.	Develop a behavioral Verilog HDL	code for generating a 150Hz pulse from 10MH	Iz clock pulse <b>(02)</b>				
2B.	An Arithmetic Unit performs the	following functions:					



where F is the output and A, B are the 1 bit inputs. Using a task for the 4 to 1 multiplexer and task for the full adder write the Verilog HDL code for the arithmetic unit

(05)

- 2C. Develop a counter to generate the sequence 8 4 2 1 8 4 2 1 ...... Using Verilog HDL Display the output on the Seven Segment display (03)
- **3A.** Given an instruction set and the corresponding relative frequency, encode using Huffman's method and calculate the redundancy. Show how this is more efficient than Block code encoding technique.

Instruction	10	I1	I2	13	I4	15	I6
Relative frequency count	0.05	0.1	0.4	0.18	0.2	0.04	0.03

**3B.** Perform **25 x - 30** using Booth's algorithm

**3C.** Differentiate between RISC and CISC.

**4A.** Given below is the register transfer logic description of control unit. Develop the control signal, Draw the processing section and the state diagram.

Declare the registers: A[4], B[4], L[4], D[4], Q[4]

Start :  $A \leftarrow 0$ ,  $D \leftarrow 0$ ,  $B \leftarrow$  In bus ;

Q←Inbus; /\* Content of B, C, & Q are positive \*/

Loop1:  $D \leftarrow B-C$ ;

If D<>0 goto loop2;

 $A \leftarrow A+1; Q \leftarrow Q-1;$ 

If Q<> 0 goto loop1;

Outbus  $\leftarrow$  D;

Loop2: Outbus  $\leftarrow$  A;

Halt;

(05)

(03)

(04)

(04)

(02)

- 4B. Determine the size of the Control Word when above Register transfer logic description implemented in Micro programming control unit and calculate the number of bits saved in each instruction using decoders (02)
- **4C.** Define and explain the following terms associated with pipeline processing

a) Speed up b) Efficiency c) Throughput

- **5A.** With a neat diagram explain 4 level Hierarchical memory system and define the following terms
  - a) Average cost per bit b) Hit Ratio c) Average access time (03)
- **5B.** Assume that main memory has 3 pages frames and consider initially all the pages are empty. Consider following stream of references

2, 3, 2, 4, 6, 2, 5, 6, 1, 4, 6

(02)

- **5C.** Realise the following function using PLA (02) a)  $F(a,b,c) = \pi M(1,3,4)$  b) F = X3X1+X2X1
- **5D.** Explain the EPROM / EEPROM Program Technology used in ALTERA (03)