Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH B.Tech (E & C) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2018
SUBJECT: DSD USING VERILOG (ECE - 2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Consider a CPLD that contains 8 macrocells in one LAB block. A function F=ABCD+A'BCD+A'BCD'+AB'CD+A'B'C'D+A'B'CD+ABCD'+A'BC'D should be implemented using CPLD. In one LAB block, there are four macrocells, each one is 3-wide OR array and remaining macrocells are 5-wide OR array. Implement the functions with minimum number of macrocells present in LAB block. Use parallel expander logic.

1B. Consider the sequential element of ACT-2 FPGA as shown in **Figure 1B**. Implement (i) Transparent low Latch (ii) Positive edge triggered D-FF.

1C. Implement F= A B'+ A C using ALTERA MAX structure. Show the connections using applicable switching elements.

(5+3+2)

2A. Implement 0101 overlapping sequence detector using ACT-2 FPGA having combinational and sequential modules.

2B. Implement 4 to 1 multiplexer using Xilinx FPGA. Specify the content of LUT.

2C. List the disadvantages of Polysilicon diffusion anti-fuse.

(5+3+2)

3A. Write a structural Verilog program for a 4:1MUX using 2:1 MUX.

3B. Write the syntax for Verilog procedural assignments. Find the output of two statements

```
S1: begin
  a = 1;
  #10 a = 0;
  #5 a = 4;
end
```

```
S2: begin
 begin
  a <= 1;
  #10 a <= 0;
  #5 a <= 4;   end
```

3C. Write a switch level Verilog code for a CMOS inverter.

(5+3+2)

4A. Write a structural Verilog program for a sequential circuit of a BCD to XS-3 code converter as shown in **Figure 4A**. Write the Verilog code for D flip-flop, 3 input NAND gate and 2 input NAND gate.

4B. Write a sequential Verilog code for 3-bit binary-to-gray code converter using function that evaluates the two-input EX-OR expression.

4C. What are user defined primitives? List the types of UDPs.

(5+3+2)

5A. Consider the circuit shown in **Figure 5A** below and apply D-algorithm. Find (i) singular cover of G1 and G3 (ii) PDC of G4 and G5 (iii) PDCF of G2.

5B. Determine the test vector for the sequential circuit shown in **Figure 5B** using ITG.

5C. Find the test vector to test single SA0 fault for the circuit shown in **Figure 5C** using PODEM technique.

(5+3+2)

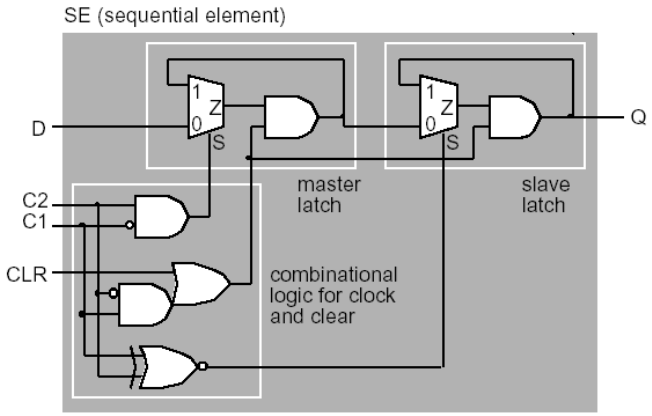

Figure 1B

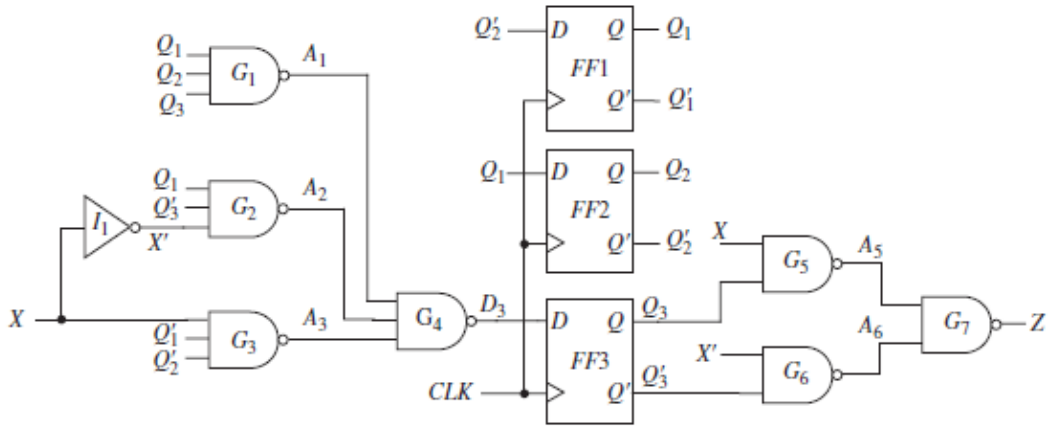

Figure 4A

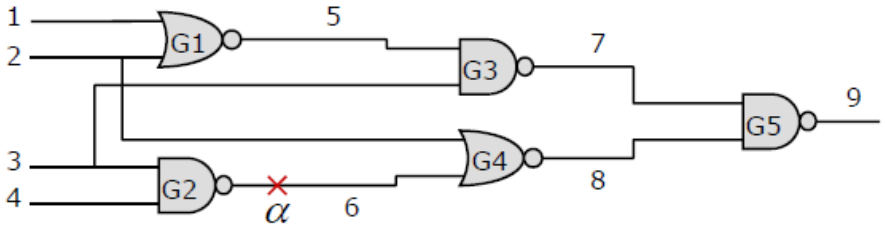

Figure 5A

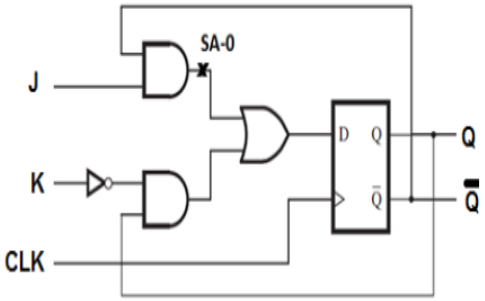

Figure 5B

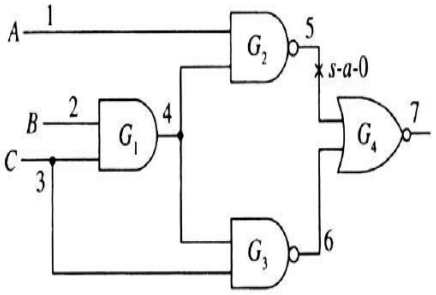

Figure 5C