Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: DSD USING VERILOG (ECE - 2204)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Map the function shown in **Figure 1A** (a) Module-1 using ACT-1 module, (b) Module-2 using PLA, and (c) Module-3 using Xilinx FPGA. Show proper I/O connections and interconnections between various IC.

1B. Implement the function F=A'B+ABC'+A'B'C using Mask Gate Array ASICs. Consider the base cell of 2:1 MUX and in one base array only 3 base cells are fabricated. Show the customization steps before and after defining the Mask.

1C. Explain Y-chart.

(5+3+2)

2A. Implement the given function with minimum number of 4-variable look-up table

$$Z = abc\bar{d}e\bar{f} + \bar{a}\bar{b}cde\bar{f} + \bar{b}cd\bar{e}f$$

2B. Implement 4-bit ring counter using ACT-2 FPGA.

2C. Two programmable interconnect (one vertical and horizontal) has to be connected using reconfigurable switching element based on MOS transistor as shown in **Figure 2C**. It has one extra floating gate.

(i) Identify the reconfigurable switching element.

(ii) Explain how reconfigurable switching element can be programed to make connection between row line and column line.

(5+3+2)

3A. Write a structural Verilog program for a 4-bit ripple carry adder using 1-bit full adder as basic building block.

3B. Write a sequential Verilog program for 4:1 MUX using CASE statement.

3C. Write a dataflow Verilog code for 4-bit Binary to Gray code converter.

(5+3+2)

4A. Write a structural Verilog program for a 4-bit ripple counter using negative edge triggered T FF signal and active high reset signal.

4B. Write a behavioural Verilog program for Universal shift register, whose operation is given in **Table 4B**.

4C. Write a dataflow Verilog program for a 4bit full adder.

(5+3+2)

5A. Consider the LFSR1 **(Figure 5A1**) acting as random sequence generator (initial content=101) and LFSR2 **(Figure 5A2**) (initial content=000) acting as signature analyser. Consider the Device-under-Test (DUT) as shown in **(Figure 5A3**). Find the signature of the faulty circuit and compare with fault free circuit.

5B. Apply SCOAP to circuit shown in **Figure 5B**. Write the formula for Controllability and observability of each individual gate.

5C. Generate a minimum set of test vectors (for inputs) to completely test an n-input NAND gate under the single stuck-at fault model for SA1. How many possible test vectors can be generated? Apply any algorithm.

(5+3+2)

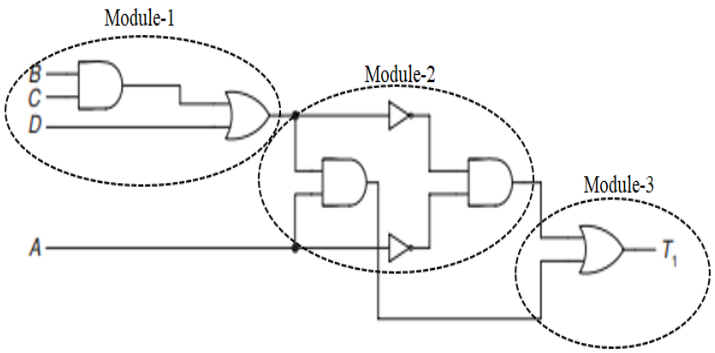

Figure-1A

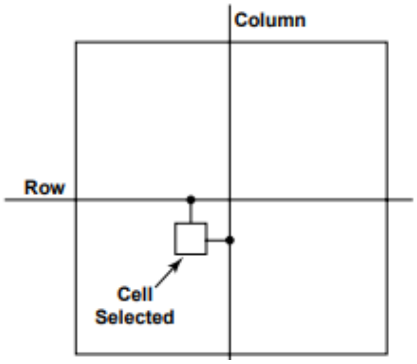

Figure-2C

Table 4B

Function	Inputs		Next State		
	S0	S1	Q(2)	Q(1)	Q(0)
Hold	0	0	Q(2)	Q(1)	Q(0)
Shift left	0	1	Q(1)	Q(0)	Right in
Shift right	1	0	Left in	Q(2)	Q(1)
Parallel Load	1	1	Input 2	Input 1	Input 0

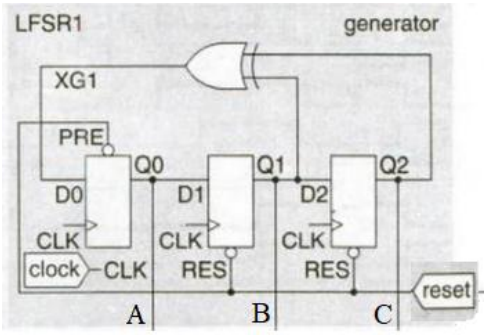

Figure-5A1

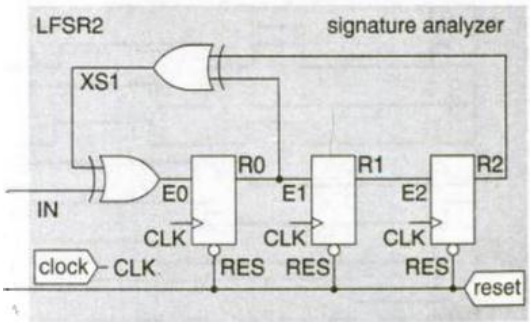

Figure-5A2

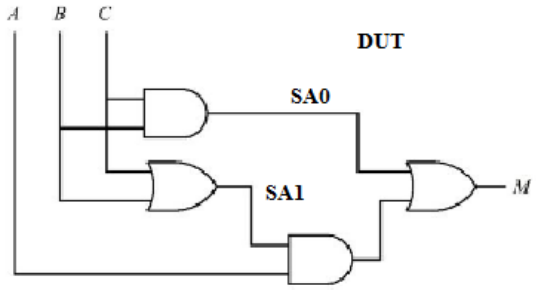

Figure-5A3

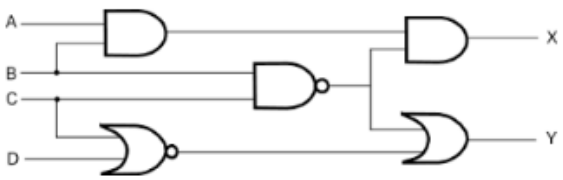

Figure-5B