Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B.Tech. DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2018
SUBJECT: ELECTRONIC PRODUCT DESIGN AND PACKAGING (ECE - 3282)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain thermal design process with neat diagram.

1B. What is product finishing? Describe any two product finishing techniques.

1C. What is product detailing? Discuss any two types of product detailing techniques.

(5+3+2)

2A. Discuss product reliability and their types. Explain the failure rate of a product with necessary plots.

2B. What is TIMs? Explain any two material used.

2C. With neat a graph explain product life cycle.

(5+3+2)

3A. Explain the chip making process with neat block diagram.

3B. Compare and contrast alpha and Beta testing.

3C. What is electronic packaging? What are the major functions of electronic packaging?

(5+3+2)

4A. Describe with neat diagram two wire bonding techniques.

4B. Explain level 1 packaging techniques in IC design.

4C. How ground and supply noise is generated? What are the remedial measures?

(5+3+2)

5A. Explain the grounding and shielding noise reduction techniques.

5B. Discuss reflection and crosstalk noise with necessary diagrams.

5C. With neat diagram, explain noise path.

(5+3+2)