Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FOURTH SEMESTER B. Tech. (E & C) DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2018
SUBJECT: I C SYSTEMS (ECE - 2202)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the circuit diagram of an emitter coupled differential amplifier. Derive an expression for CMRR. Assume identical transistors with β=100. Compute CMRR in dBs if R_C=2.2kΩ, R_E=4.7 kΩ. Assume the supply voltage ± 10V and V_{BE}=0.7V

1B. Design a current mirror circuit to provide a current of 2.2mA. Derive the relevant equations used. Assume the supply voltage ± 10V and V_{BE}=0.7V.

1C. Discuss how the input resistance of an Op-Amp is measured experimentally. Find the input resistance of an Op-Amp from the following observations: (i) output is 2V when input is directly connected between the two input terminals of Op-Amp and (ii) output is 1.99277V when series resistance of 10kΩ connected at both the input terminals.

(5+3+2)

2A. Draw the input/output voltage waveforms of an Op-Amp which has gain of 100dB, Slew rate is 0.5V/µsec in each of the following cases: Assume supply voltage ± 10V and zero output offset voltage.

(i) $V_{inverting} = 40\sin(314t)$ µV and $V_{non-inverting} = 10\sin(314t)$ µV

(ii) $V_{inverting} = 50\sin(314t)$ µV and $V_{non-inverting} = 500\sin(314t)$ µV

(iii) $V_{inverting} = 10\sin(3140000t)$ µV and $V_{non-inverting} = 0$ V.

(iv) $V_{inverting} = 0$ V & $V_{non-inverting} =$ Square wave: 1 V for 80µsec and -1 V for 20 µsec.

2B. Draw the circuit diagram of a voltage to current convertor with grounded load and derive the expression for the output.

2C. Design an inverting Schmitt trigger circuit for V_{UT} = 4V, V_{LT} = -4V and ± V_{sat} = ±10V

(5+3+2)

3A. With the help of a circuit diagram and waveforms explain the working of a full wave precision rectifier. Derive the expression for the output voltage.

3B. Design an Op-amp based notch filter with notch frequency of 50 Hz and quality factor of 10. Plot the frequency response. Assume capacitance value of 100nF.

3C. List the merits and demerits of an active filter.

(5+3+2)

4A. Design a Butterworth filter which allows signal of frequency ranging from 400 Hz to 2kHz. The filter must have a roll-off rate of 40 dB/decade and pass band gain of 10. Assume capacitance value of 100nF.

4B. Design a circuit which produces rectangular pulses of frequency 1kHz with 30% duty cycle and amplitude 5V using 555 timer. Select capacitance value of 100nF.

4C. Draw the circuit diagram of monostable multivibrator using 555 IC. Derive the expression for the pulse width of the output signal.

(5+3+2)

5A. Draw the circuit diagram of a 4-bit R-2R resistor type DAC. Determine the output when

(i) $b_3b_2b_1b_0$ = 0100 (ii) $b_3b_2b_1b_0$ = 1000. Select R = 10 kΩ, R_F = 20 kΩ, Logic 0 = 0V and Logic 1 = 5V.

5B. In the VCO, the biasing voltage = 10V, V_{CC} = 12V, R_T = 15 kΩ, C_T = 0.001μF. Compute

(i) the free running frequency.

(ii) if the modulating voltage is varied from 7V to 8V, find the range of output frequency.

5C. Explain how an analog signal of 5.5V gets converted into 8-bit digital output, using successive approximation type ADC, if V_{FS} = 10 volts.

(5+3+2)