Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

IV SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

END SEMESTER EXAMINATIONS, APRIL 2018

COMPUTER ORGANISATION AND MICROPROCESSOR SYSTEMS [ICT 2202]

REVISED CREDIT SYSTEM

(19/04/2018)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer ALL the questions.
- Missing data, if any, may be suitably assumed.

1A. Explain paging and segmentation memory management techniques with neat block diagrams. 5

1B. Explain the following addressing mode of 8086 microprocessor with an example for each:
i. Variable port ii. Register Indirect iii. Based indexed 3

1C. If the physical branch address is 5A230H when CS = 5200H, what is the physical address if CS is changed to 7800H? 2

2A. Explain the following instructions with an example for each:
i. XLAT ii. IDIV iii. JLE iv. SAR v. SCASB 5

2B. Draw the block diagram of 8254 and answer the following:
i. Find the configuration for 8254 if the control register is programmed as follows:
MOV AL, 36H
OUT 97H, AL
ii. Program, Counter 2 to operate in mode 3 with binary count, to divide CLK 2 by number C26AH. Also, find the frequency of OUT 2 for this configuration, if CLK 2 = 1.8 MHz. 3

2C. Explain the priority in which 8086 services the interrupts if two or more interrupts occur at the same time. 2

3A. Given M = $17_{(10)}$ and Q = $-16_{(10)}$, perform multiplication using Booth's Algorithm indicating all the steps. 5

3B. Assume a 3 x 8 matrix keyboard is interfaced to 8086 using a programmable peripheral interface 8255 working in mode 0. Write an 8086 procedure that detects a key press and returns the keycode in the register BL. 3

3C. Assume a system's memory has 128M words. Blocks are 64 words in length and the cache consists of 32K blocks.
i. What are the sizes of the tag, set, and word fields assuming a set associative cache mapping scheme with 4 blocks/set?
ii. Also specify the first four block numbers of main memory in ascending order that map to set 0. 2

4A. Design the Microprogrammed controller for the algorithm given below:

```
Declare registers A[4], M[4],Q[5], L[3];
Declare buses Inbus[4], Outbus[4];
Start:  A←0, M←Inbus, L←4;
        Q[4:1]←Inbus, Q[0]←0;
Loop:   If Q[1:0]=01 then Goto Add;
        If Q[1:0]=10 then Goto Sub;
        Go to Rshift
Add:    A←A+M;
        Go to Rshift
Sub:    A←A-M;
Rshift: ASR(AQ), L←L-1;
        If L<>0 then Goto Loop
        Outbus=A;
        Outbus=Q[4:1];
Halt:   Go to Halt;
```

5

4B. Treat the concatenation of the contents of DX:AX as a 32-bit number and write a program that puts the bit position number of the first bit containing a 1 from the least significant bit position, in register BL. 3

4C. Explain the following pins of 8086 microprocessor:
i. ALE ii. RESET 2

5A. Draw a neat diagram of 8086 architecture and explain different parts of Execution Unit. 5

5B. With neat diagrams, explain polled and daisy chain techniques for servicing multiple interrupts. 3

5C. Explain cycle - stealing and interleaved DMA. 2