Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

II SEMESTER M.TECH. (POWER ELECTRONICS AND DRIVES)

END SEMESTER EXAMINATIONS, APRIL 2018

SUBJECT: EMBEDDED SYSTEM DESIGN [ELE 5236]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 25 April 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Support all your programs with relevant comments

1A. Discuss the necessity of benchmarks to assess the processing power of a processor. Describe the Dhrystone benchmark in detail and mention the benchmark developed by EEMBC to replace the Dhrystone benchmark. ***(03)***

1B. Write PIC16f877 program to configure RB2 pin as input pin and RB4 as output pin. Check the status of RB2, wait till it is zero (low); when it is low, make RB4 pin high, and make it low again after a suitable delay (Port 'B' is in RAM bank 1). Determine the time delay obtained, if fosc = 20MHz. Assume all instructions to take 4 clock cycles for execution. ***(03)***

1C. Give the bitwise details of CPSR register of ARM7TDMI and explain the function of all the used bits.

Consider the ARM7 instruction **ADDS R0,R1, R2**

If (R1) = 0x80003500, (R2) = 0xC450E050. Determine the value of R0 register and all the four condition flags, after the execution. ***(04)***

2A. List and describe the different types of stack in ARM7TDMI processor. Mention the ARM7 instructions for push and pop operations in each of these stack type. ***(03)***

2B. Write an ARM7TDMI subroutine to determine the parity of a 32 bit number passed to subroutine through 'R0' register. In case of even parity, return 01 in 'R1' register and return '02' in case of odd parity. If the number is '0', return back (without attempting to determine parity) with 00 in 'R1' register. ***(03)***

2C. Write ARM7TDMI instructions to do the following operations

i. Obtain the 2's compliment of a 16 bit number available in 0x00009000, 9001 and store the result in same locations.
ii. Enable FIQ interrupt, without modifying other bits of CPSR register.
iii. Change the mode of operation to user mode, without modifying other bits of CPSR register. ***(04)***

3A. Show the interfacing circuit to interface two common anode seven segment display devices to pins p10 to p17 and p20 to p27 of mbedNXPLPC1768 microcontroller. Write a 'C' program to display numbers 00 to 99 at the display devices continuously with a delay of 1.8 seconds. ***(03)***

3B. Explain the following with respect to cache memory

i. Necessity and uses of cache memory.
ii. FIFO replacement policy.
iii. Write through and write back techniques. ***(04)***

3C. With the help of a relevant timing diagram, explain PCI bus protocol for memory read operation to transfer four '24' bit data in the data field. Assume that no wait cycles are required in case of data '1' and '3'. Target requests for one wait cycle during data '2' and initiator requests for two wait cycles during data '4'. ***(03)***

4A. i. Show the connection diagram to connect single master and multiple slave devices to SPI serial communication bus and describe the role of all the SPI bus signals.
ii. Describe the SPI communication protocol. ***(03)***

4B. Write a 'C' program for PIC16f877 to configure MSSP in I2C master mode to transmit data bytes 29H, 3AH and 5CH to a slave device with address 6BH at a baud rate of 1Mbps. Assume fosc = 16MHz. ***(03)***

4C. List the various fields involved in data transfer over CAN serial communication bus and describe them clearly. ***(04)***

5A. i. List the different types of ADCs and compare them with respect to conversion time, accuracy and cost.
ii. Answer the following with respect to on chip ADC of PIC 16f877.
a. If V_{ref+} =4V and V_{ref-} = 0V, determine the resolution.
b. With reference voltages as given in I, if analog input voltage is 3.7V, determine the digital output and hence the values of ADRESH and ADRESL registers with left justified result. ***(03)***

5B. i. Describe the salient features of IRDA Wireless communication protocol; list the various standards and data transfer rates supported by IRDA.
ii. With the help of a relevant diagram, describe the functions of IR encoder / decoder and IR transceiver in realizing SIR communication. ***(04)***

5C. With the help of a relevant diagram, describe the priority arbitration scheme for expanding the number of interrupts to a processor. List the merits and demerits of this scheme by comparing it with daisy chain arbitration scheme. ***(03)***