Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.Tech (DEAC & ME) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: CAD TOOLS FOR VLSI DESIGN (ECE-5234)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Find the essential prime implicant for the set of prime implicants F={C_1, C_2, C_3, C_4} where $C_1 = \overline{x_1}\,\overline{x_3}\,\overline{x_4}$, $C_2=x_1x_2$, $C_3=x_3x_4$, $C_4 = x_2\,\overline{x_3}\,\overline{x_4}$ using ESPRESSO algorithm.

1B. Determine the prime implicants for the following function using Iterative consensus method

F=$\sum$m(0,1,2,3,4,7)

1C. Draw control and data flow graph (CDFG) for executing the following sequential statements x=a*b, y=c+d, if x<y then z=y-x else z=x-y.

(5+3+2)

2A. Implement the given function using ACT3 S module. Find the minimum number of logic modules required to implement. D1= $\overline{X} + Y_1$, D2= $X\overline{Y_2}$ + $\overline{X}\,\overline{Y_1}$, Z=$XY_1$

2B. Implement the following expression using PAL(Altera max FPGA) architecture with 3 wide OR array plane (using shared logic expander)

$$F= \overline{A}CD + \overline{B}CD + AB + B\overline{C}$$

2C. Explain Y Chart

(5+3+2)

3A. Apply Hu algorithm for the given graph shown in Fig.Q3. Calculate latency using ASAP algorithm. Assume d=1, P(0)=1, P(1)=3, P(2)=4, P(3)=2, P(4)=2. Determine the resource constraints using Hu algorithm. Draw the scheduled graph with resource constraints. All the operations has unit execution delay

3B. Perform LIST-L scheduling algorithm for the above sequencing graph in Fig.Q3. Draw the scheduled graph with resource constraints.

3C. Define scheduling. What are all the different types of scheduling?

(5+3+2)

4A. Find the test vector using Boolean difference method for the circuit shown in Fig.Q4A

4B. Construct ROBDD for the synchronous counter that counts in the sequence 0, 2, 4, 5, 6…. Also perform ITE algorithm. Show all the iterations till it becomes a single variable.

4C. Define the term Design for Testability (DFT). What are the different methods of DFT?

(5+3+2)

5A. Find the test vector using D algorithm by considering SA_0 fault at node α for the circuit shown in Fig.Q5A

5B. Determine the test vector for the sequential circuit shown in Fig.Q5B using ITG.

5C. Draw the stick diagram for 2 input XOR gate

(5+3+2)

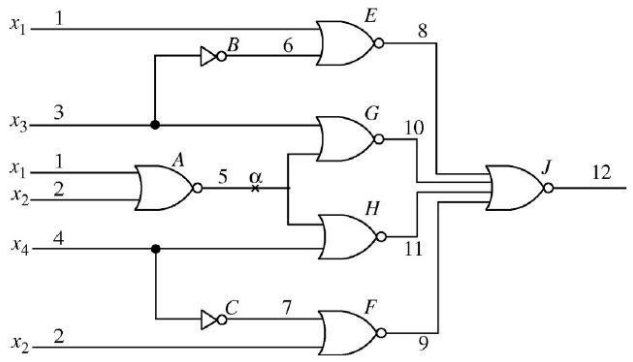

Fig. Q5A

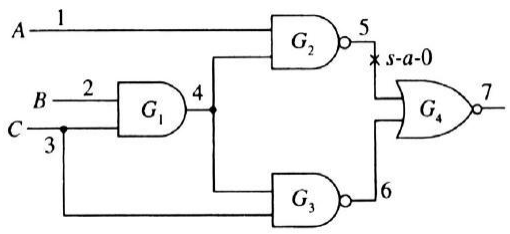

Fig Q4A

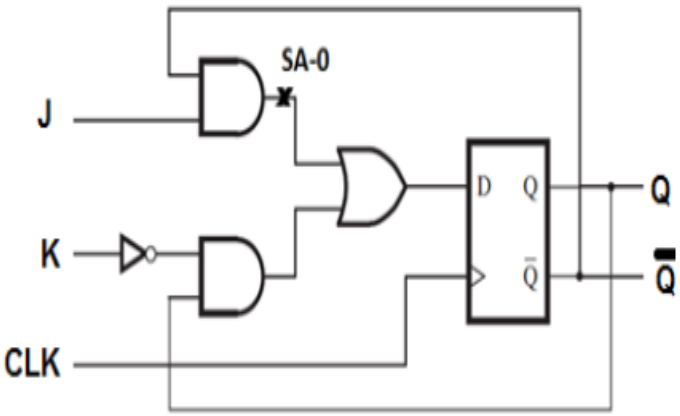

Fig Q5B

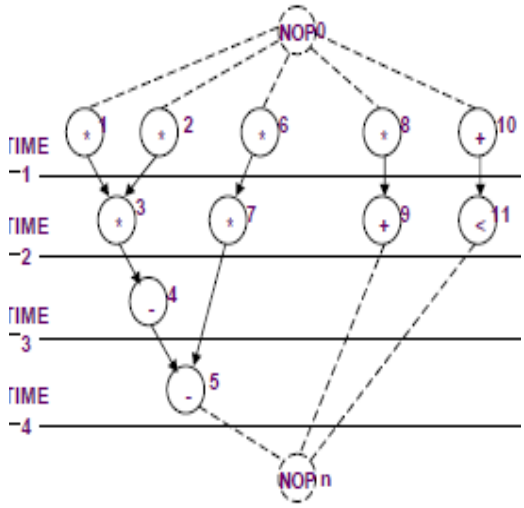

Fig Q3