Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND M.TECH DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: VLSI TESTING & TESTABILITY (ECE - 5259)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Apply FAN to following circuit 1A to find the test vector.

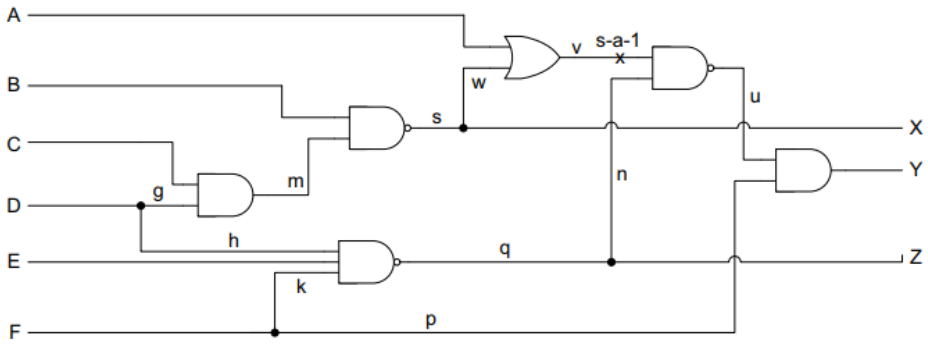

Figure 1A.

1B. Apply Robust Delay Test to the circuit 1B to find the test vector. Consider falling transition at B.

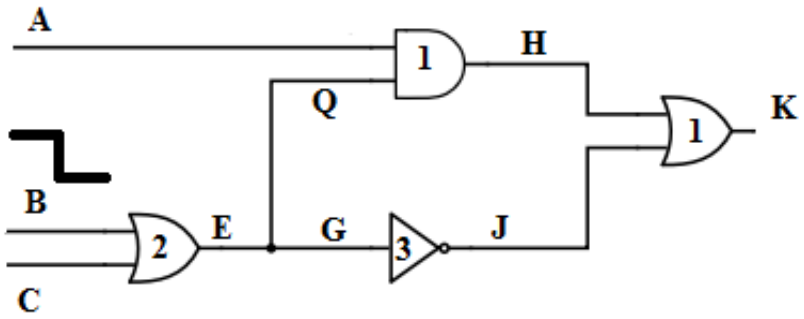

Figure 1B.

1C. Using test data analysis a chip production process has been characterized with fault density, f=1.45 faults/sq. cm, and fault clustering parameter,β=0.11. Given that the fault coverage of tests is 95%, calculate the defect level for a chip of 1 sq. cm area.

(5+3+2)

2A. In the circuit FIGURE 2A, suppose that we want to obtain a test vector for the c1 s-a-0 fault. (i) Show that path sensitization through gates G5 and G8 or G6 and G8 does not yield such a test vector. (ii) Obtain a test vector by considering alternative path/paths. Use only D-algorithm for both cases.

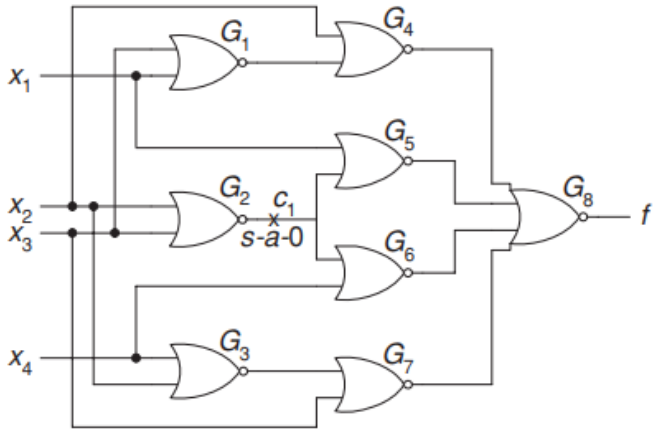

Figure 2A.

2B. Find the test vector for the circuit shown in FIGURE 2B using ITG method.

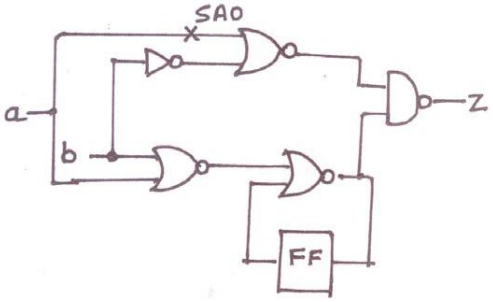

FIGURE 2B.

2C. Explain C-Temporarily Critical with respect to circuit 2C.

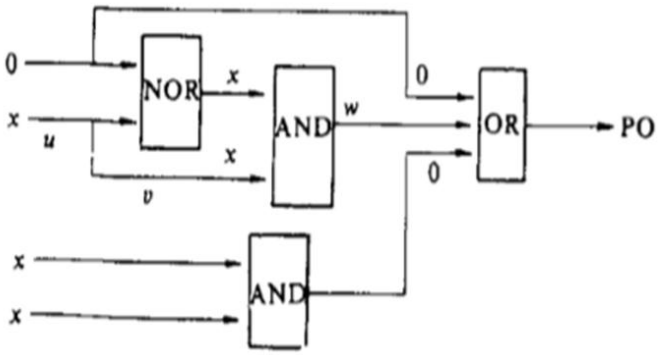

FIGURE 2C.

(5+3+2)

3A. For the circuit shown in Figure 3A. (i) find test vector using PODEM. (ii) find vanishing D-frontier gate if any. (iii) Is fault redundant? (iv) Mark X-path.

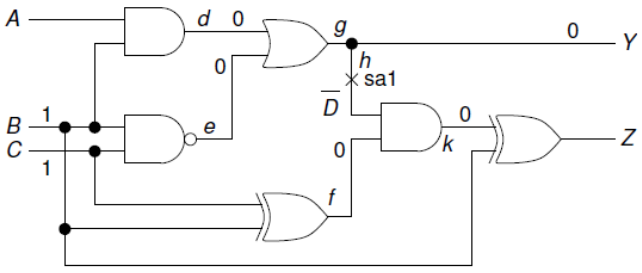

Figure 3A

3B. Find the Reed-Muller coefficient for circuit shown in Figure 3B for faulty and fault free circuit. Consider SA1 at input B.

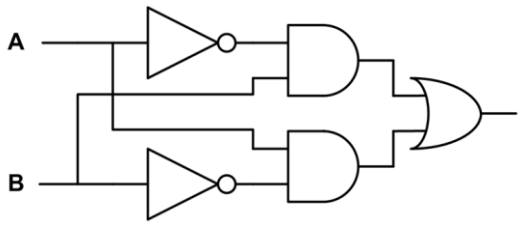

Figure 3B.

3C. The test vector (A, B, C, D, E, F , G, H) = (0, 1, 1, 1, 1, 1, 1, 1) was applied to the circuit shown in Fig. 3C and output f indicated an error. What are the single stuck-at faults in this network that could cause the output to be erroneous?

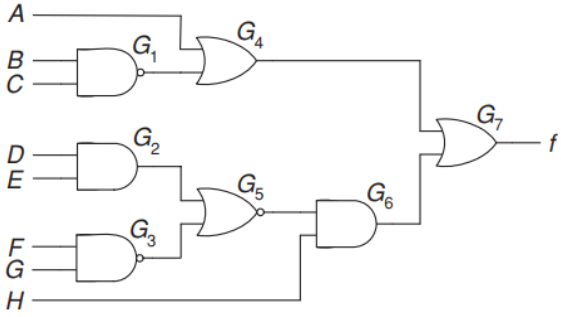

Figure 3C.

(5+3+2)

4A. Apply SCOAP to circuit shown in Figure 4A.

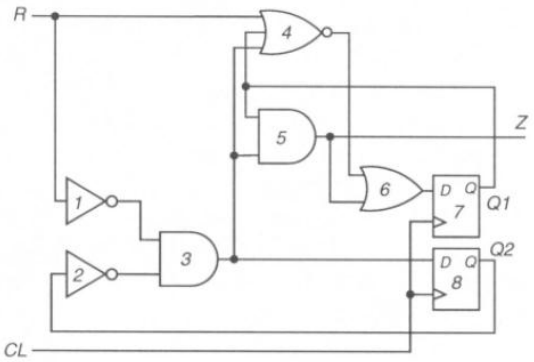

Figure 4A

4B. Consider the Roth's five valued algebra and possible two input basic gates. Find (i) forward implication value of possible two input basic gates if one of its input is at D and (ii) forward implication table in the format shown in Figure 4B for AND operation. (iii) backward implication value of two input gates

	0	1	X	D	D'
0					
1					
X					
D					
D'					

Figure 4B

Figure 4B.

4C. Implement a standard LFSR for the characteristic polynomial $f(x)=x^8+x^7+x^2+1$ .Write the system of equations with the *companion matrix* for this LFSR.

(5+3+2)

5A. The crash of Japan Airlines Flight 123 on August 12, 1985, is the single-aircraft disaster with the highest number of fatalities.520 people died on board a Boeing 747. Investigator have found that control circuit (circuit under Test) shown in Figure 5A has fault in B SA0, B SA1, f SA0 and f SA1. Suggest a scheme with explanation and calculation, how the above faults can be identified. Initial content of Pattern generator is 001 and response compactor is 000.

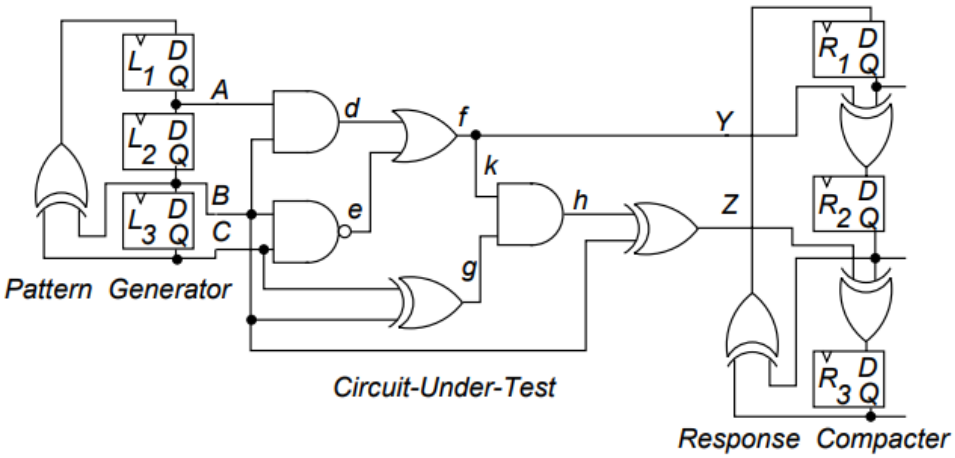

Figure 5A.

5B. For the circuit shown in Figure 5B, is there any test possible to detect the shorted inverter. Use only Boolean difference technique.

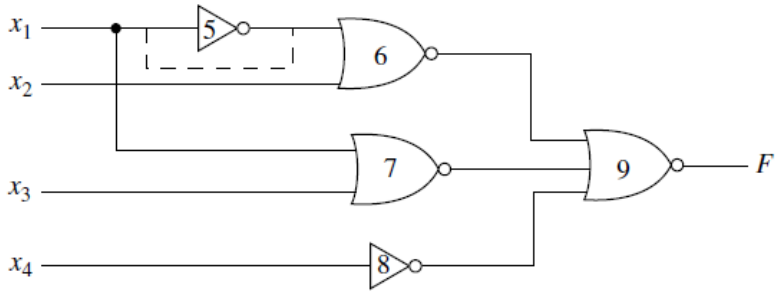

Figure 5B.

5C. (i) How many mandatory extra pins does each device need to have relative to non-boundary scan environment and name the signals associated with each of these pins?

(ii) Are the power and ground pins placed in the boundary scan data register?

(5+3+2)