


SECOND SEMESTER M. TECH (O E) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: ARM PROCESSOR AND APPLICATIONS (ECE - 5233)
TIME: 3 HOURS
MAX. MARKS: 50
Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

- 1A. LPC 2129 target board is in ARM state. Write a program to flash all LEDs which are connected to IODIR register starting from P1.16 to P1.31. Use maximum time delay for flashing. Repeat the sequence.
- 1B. With a neat block diagram, describe how ARM core is used in an VLSI ISDN Subscriber Processor
- 1C. With diagrams, explain different types of cache, based on its architecture
(4+4+2)
- 2A. Draw a neat diagram of ARM Programmer model and explain each functional component.
- 2B. Consider ARM processor to be in ARM state. Write a program to add two 96 bit numbers stored in memory locations pointed by registers r0 and r1. Store the sum in memory location pointed by register r2. Do not ignore carry.
- 2C. Explain Polling I/O strategy with algorithm and code used for implementation.
(4+4+2)
- 3A. Explain 4KB Cache memory system with necessary diagrams. Discuss role of cache controller.
- 3B. Consider ARM processor to be in ARM state. How multiple load store operations are carried out in ARM processor? Tabulate all addressing modes and explain with an example.
- 3C. Describe working of FPA 10 processor.
(4+4+2)
- 4A. Explain AMBA based system emphasizing on bus transfers, slave, APB, AHB and ARM multiplexed bus scheme.
- 4B. What are the different types of arithmetic and logical instructions in ARM? Explain each with one example.
- 4C. Discuss ARM address register structure.
(4+4+2)
- 5A. Explain the significance of a barrel shifter in executing various operations in ARM. List all instructions associated with it with few examples.
- 5B. Discuss non nested interrupt controller with necessary flow charts and code.
- 5C. Explain the process of enabling and disabling of IRQ and FIQ interrupts.
(4+4+2)