Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.Tech. (ME) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: CMOS MIXED SIGNAL DESIGN (ECE - 5222)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. [i] Justify the distortion improvement in fully-differential circuits as compared to single ended circuits.

[ii] With a schematic circuit, explain the working and the ideal properties of CFOA.

1B. Give fully differential OTA-C implementation of ladder filter given in **FIG. 1B**.

1C. With a block diagram explain the circuit realization of comb filter using a suitable active device.

(5+3+2)

2A. Give the circuit diagram for passive RLC band-pass biquad and then realise voltage mode OTA-C equivalent circuit. Derive the expression for transfer function for both circuits. Give the expression for pole frequency and pole-Q. Obtain expression for single parameter sensitivity as applicable.

2B. Show that integrators can be used to realize second-order oscillators. Discuss two op-amp based oscillator circuit using Deboo integrator. Derive the expression for frequency of oscillation

2C. Discuss OTA-C simulation of parallel LC resonator as a series impedance element with expressions for L and C.

(5+3+2)

3A. Describe the different non-ideality macro models of OTA. Discuss the non-ideality of OTA as applied to the circuit in **FIG. 3A**.

3B. Find the expression for Z_{in} in terms of component values for the circuit shown in **FIG. 3B**. Give your comments.

3C. [i] Illustrate how virtual ground can be established in an op-amp based inverting amplifier.

[ii] Define the term total harmonic distortion (THD).

(5+3+2)

4A. Give the circuit diagram of 6-bit charge scaling DAC using a split capacitor array. Find the value of output voltage if $d_5 d_4 d_3 d_2 d_1 d_0 = 100000$. Discuss the layout considerations for the capacitor array used in charge scaling DAC.

4B. Discuss the merits and demerits associated with switched capacitor circuits.

4C. Analyze the OTA-based circuit given in **FIG. 4C** and give your comments.

(5+3+2)

5A. [i] Give an account of nonlinearity errors associated with DACs.

[ii] Give the op-amp based circuit for grounded negative resistance simulation.

[iii] Design a OTA-C voltage-mode first-order all-pass filter for a cut-off frequency of 10 MHz.

5B. Show how Miller's theorem can be used to realize negative capacitance circuit using OTA.

5C. Explain the significance of fractance device.

(5+3+2)

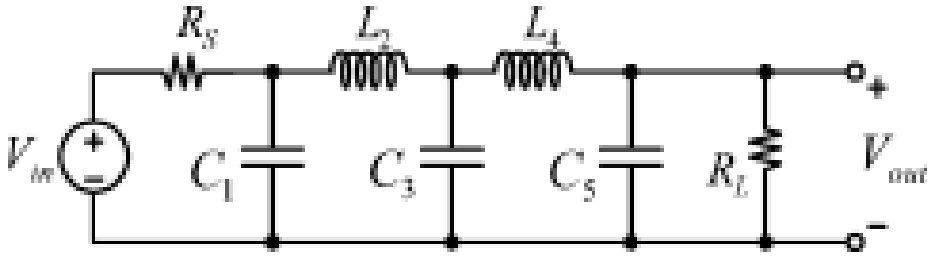

FIG. 1B

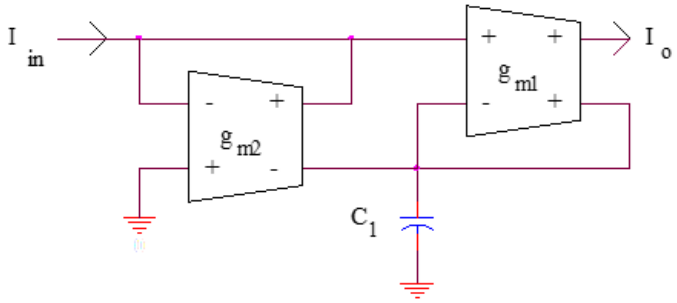

FIG. 3A

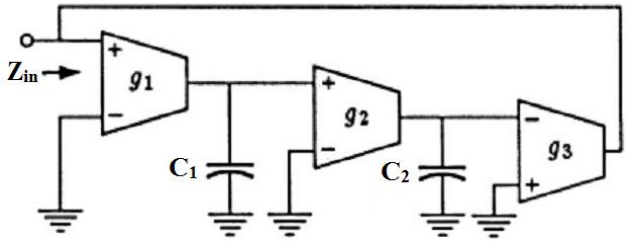

FIG. 3B

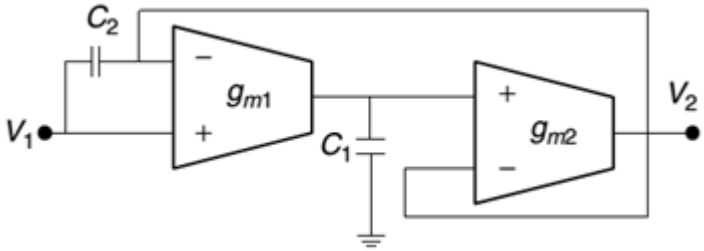

FIG. 4C