Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M.Tech. (ME) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: LOW POWER VLSI DESIGN (ECE - 5221)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss the need for level converters in VLSI circuits and highlight the problems faced in using level converters in VLSI design. Also explain the ways to mitigate them.

1B. For a CMOS inverter a square waveform is fed at its input with rise and fall times of t_r = 2 ns and t_f = 3 ns. If C_{ox} = 10 fF/μm^2, calculate the average short circuit power dissipated. Assume that the short circuit current waveform is triangular, and flows for the entire duration of t_r and t_f.

(W_P/L_P = 4/0.5 and W_N/L_N = 2/0.5, and operating with V_{DD} = 3.3V. Assume μ_p = 130 cm^2/V.sec, μ_n = 545cm^2/V-Sec. V_{tn} = 0.8V, V_{tp} = -0.8V.)

1C. List the factors that makes power an important design specification in VLSI.

(5+3+2)

2A. With the help of suitable examples and HDL coding illustrate how dynamic power can be reduced in FSMs.

2B. With the help of an example explain bus segmentation for achieving low power and discuss its salient features.

2C. List the demerits of employing low swing buses in VLSI.

(5+3+2)

3A. Discuss crosstalk in VLSI circuits and it's impact on the power dissipation and delay. Also, explain the techniques used to reduce crosstalk.

3B. Estimate the intrinsic wire delay of a Cu wire of length 10mm above a M1 ground plane with SiO_2 dielectric in 90nm CMOS technology, with thickness, width and height all equal to 6λ. Assume: ρ = 30 ohm-um, c = 0.10 fF/μm. What will be the delay if a buffer with 200ps delay is inserted at the centre of the line? Calculate the optimum segment length needed for getting the optimum delay for a buffer delay of 200ps.

3C. List the process level techniques employed for leakage reduction.

(5+3+2)

4A. Explain MTCMOS and VTCOMS techniques for reducing leakage power and compare them.

4B. The circuit shown in **Figure 4B,** is designed using 65nm CMOS technology using low threshold transistors. Each gate has a delay of 5ps and a leakage current of 10nA. Given that a gate with high threshold transistors has a delay of 10ps and leakage of 1nA, optimally design the circuit with dual-threshold gates to minimize the leakage current without increasing the critical path delay. What is the percentage reduction in leakage power? What will be the leakage power reduction if a 30% increase in the critical path delay is allowed? Calculate.

4C. Compare active leakage and standby leakage in VLSI circuits.

(5+3+2)

5A. Taking a low power processor or microcontroller as an example, explain the low power features and techniques employed in processor design.

5B. Discuss the adiabatic principle using suitable expressions. What are the merits and challenges involved in adiabatic logic? List and explain.

5C. List the salient features of predictive technique for dynamic power management.

(5+3+2)

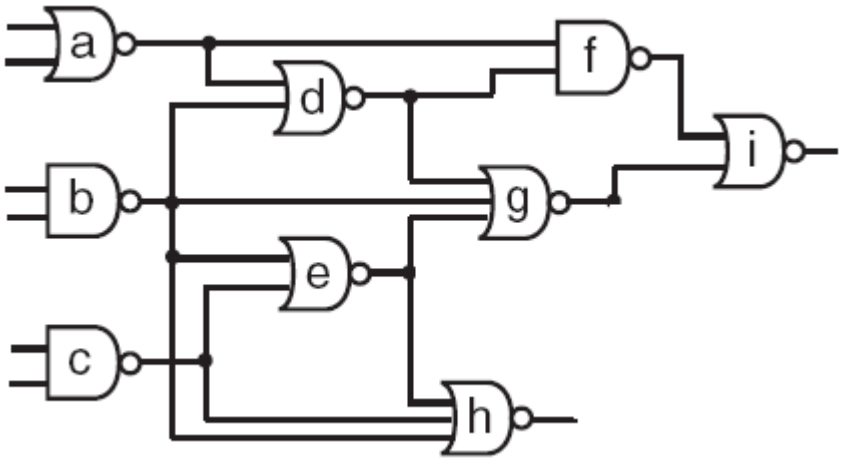

Figure 4B