Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER M. Tech. (DEAC/ME) DEGREE END SEMESTER EXAMINATION APRIL-2018)

SUBJECT: VLSI PHYSICAL DESIGN AND VERIFICATION (ECE - 5258)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer ALL the questions.
- Missing data may be suitably assumed.

1A. For the circuit shown in Fig. 1A, assume the delay through the Register ($t_{clk\text{-}Q}$ = 0.6ns) and the delay through each block has been indicated inside the boxes. Assume that the registers are positive edge triggered, have a set up time t_{Su} of 0.4 ns and t_{hold} of 0.5 ns,

(a) Determine the minimum clock period disregarding the clock skew.
(b) Repeat part (a), factoring in a nonzero clock skew: $\delta = t'_\theta - t_\theta$ = 1ns.
(c) Repeat part (a), factoring in a non-zero clock skew: $\delta = t'_\theta - t_\theta$ = 3ns
(d) Repeat part (a), factoring in a non-zero clock skew: $\delta = t'_\theta - t_\theta$ = -2ns
(e) Derive the maximum positive clock skew (i.e. $t'_\theta > t_\theta$) that can be tolerated before the circuit fails.
(f) Derive the maximum negative clock skew (i.e. $t'_\theta < t_\theta$) that can be tolerated before the circuit fails.

1B. Why circuit partitioning is necessary? Apply the Kernighan and Lin (KL) algorithm for Fig. 1B to get the best possible solution. For the given initial partition {aef, bcd}, assume clique based method to assign the weight and the break ties in lexicographical order.

(5+5)

2A. Consider the following sequence pair: SP1 = (63528417, 17452836) with the dimension of modules 1 through 8 are {(5,3), (2,3), (6,3), (2,5), (6,2), (5,1), (3,8), (6,3)}. Do the following,

(a) Draw the HCG and find the width of floorplan
(b) Draw the VCG and find the width of floorplan
(c) Finally draw the floorplan and place the lower left corner of each block to the lower left corner of its room.

2B. Briefly explain the order of execution of scheduling semantics used in Verilog IEEE standards.

2C. Draw the environment of RTL simulation and synthesis for digital design and specify all the inputs and outputs?

(5+3+2)

3A. Given the following netlists with six cells [C1, C2, C3, C4, C5, C6] and six nets N1 = {C1, C3, C4, C6}, N2 = {C1, C3, C5}, N3 = {C1, C2, C5}, N4 = {C1, C2, C4, C5}, N5 = {C2, C5, C6} and N3 = {C3, C6}. Consider C1 as seed block, find the order of blocks using Linear Ordering Algorithm (LOA).

3B. Explain the "mesh topology" for power and ground routing used in digital design systems with a neat diagram. M1 to M8 metal layers are given for routing realization.

3C. Perform the nine zone method to do the pin assignment of the block M to block A, B and C for the below given Fig. 3C.

(5+4+1)

4A. Apply the Zero skew algorithm to find the final point of clock source to connect the four sinks points located at P (8,0) with capacitance (C) = 16F, Q (22,6) with C = 10F, R (0,10) with C = 1F and S (5,15) with 2F. Assume resistance per unit length $\alpha = 0.1\ \Omega$ and capacitance per unit length is $\beta = 0.2$ F.

4B. Briefly explain formal verification method using the block diagram.

4C. What is doglegging in channel routing? Apply Doglegging in Fig. 4C to do the channel routing?

(5+3+2)

5A. Briefly explain the principle of property based verification using block diagram? Consider the specification of two-way arbiter having request lines r1, r2, grant lines g1, g2 and clk. Some properties of the arbiter are as follows,

1. Either g1 or g2 is always false (mutual exclusion)
2. Whenever r1 is asserted, g1 is given in the next cycle.
3. When r2 is the sole request, g2 comes in the next cycle.
4. When none are requesting, the arbiter parks the grant on g2.

Do the property checking, If RTL designer has the implementation as shown in Fig. 5A.

5B. Write the pseudo code for unconstrained Left Edge Algorithm (LEA).

5C. Compare FPGA and ASIC in terms of NRE cost.

(5+3+2)

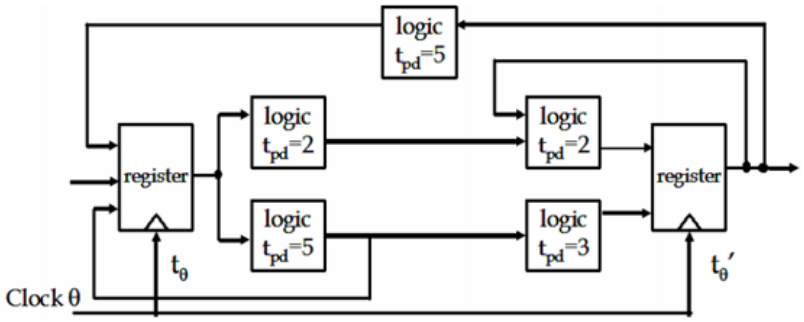

Figure 1A

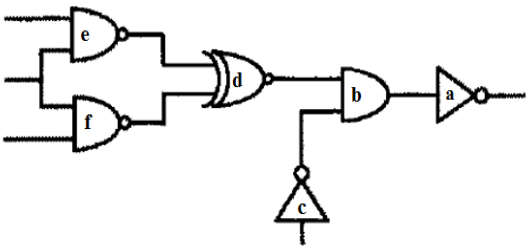

Figure 1B

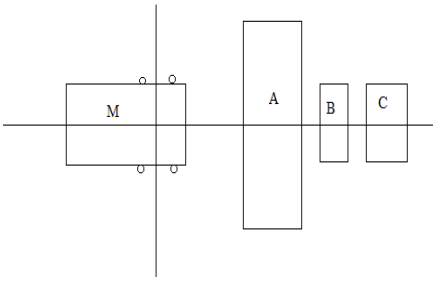

Figure 3C

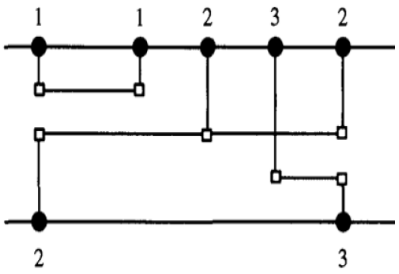

Figure 4C

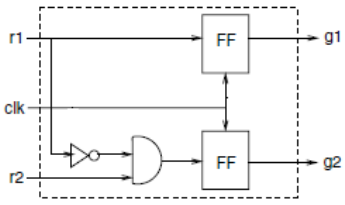

Figure 5A