# Question Paper

Exam Date & Time: 24-Apr-2018 (10:00 AM - 01:00 PM)

## MANIPAL ACADEMY OF HIGHER EDUCATION

**SCHOOL OF INFORMATION SCIENCES (SOIS)**
**FIRST SEMESTER ME - (EMBEDDED SYSTEMS)**
**DEGREE EXAMINATION- APRIL 2018**
**Tuesday, April 24, 2018**
**Time : 10:00am to 1:00pm**

**Advanced Computer Architecture [ESD 611]**

**Marks: 100** **Duration: 180 mins.**

## Answer all the questions.

1) A. Explain interface and implementation with reference to levels of abstraction in computer architecture with an example (10)

B. Write instruction using 3, 2 and 1 address method for the following

Y = ((A - B) /C) + ((D * E) + F)

2) In a computer instruction format, the instruction length and the size of an address field are 11 and 4 bits respectively. Check that is it possible to have (10)

7 two-address instruction
15 one-address instruction
16 Zero-address instruction by showing relevant steps

3) What is a combinational shifter? Write the block diagram, internal organization and truth table of a typical 4 X 4 combinational shifter. (10)

4) Explain the division using non restoring algorithm with the flowchart and show 11/4 (10)

5) Consider the following Algorithm (10)

```
Declare Register A[8], B[8], C[8];
Start:  A ← 0;
        B ← 00001010;
Loop:   A ← A + B;
        B ← B – 1;
        If B! = 0 then go to Loop
        C ← A;
Halt:   End
```

Propose a block schematic of the microprogrammed control unit, provide the state diagram and obtain the control words required in the control memory

6) Design and implement a combinational circuit that will work as follows (10)

| S1 | S0 | F |
|---|---|---|
| 0 | 0 | A plus B |
| 0 | 1 | Shift left A |
| 1 | 0 | A plus B plus 1 |
| 1 | 1 | Shift left (A) + 1 |

**Note:** A and B are 4 bit operands

7) Explain the different registers available in ARM7 (10)

8) Explain the following instructions in ARM7: (10)
SBC, SUBGT, TST, LDR, STMEA

9) Explain the SWP, Branch and Branch & Link instructions in ARM with relevant example (10)

10) Write short notes on data hazards and structural hazards (10)

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