Question Paper

Exam Date & Time: 23-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER Master of Engineering - ME (EMBEDDED SYSTEMS)
DEGREE EXAMINATION APRIL 2018
Monday, 23 April 2018
Time : 10:00 am to 1:00 pm
Digital Signal Processing [ESD 602]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1) Find the 8-point DFT of $x(n) = 2^n$ for n = 0 to 7, using DIT-FFT algorithm. Using this result, find the DFT of the sequence y(n) where $y(n) = 2^{(n+4)}$ for n = 0 to 3 and $y(n) = 2^{(n-4)}$ for n = 4 to 7 (10)

2) Realize the following system functions using Direct form-I, Direct form-II, Cascade / Parallel form (10)

$$H(z) = [(z^{-2} + z^{-1} + 1) / (z^{-2} - 1)] + [(z^{-1} + 1) / (z^{-2} + 2z^{-1} + 2)]$$

3) Implement the frequency sampling structure for the following impulse responses (10)
$h(n) = 2\delta(n) + 0.5\delta(n-1) + 0.5\delta(n-7)$

4) Design an FIR linear phase lowpass filter using windows to meet the following specifications. (10)

$$0.99 < |H(e^{jw})| \leq 1.01; \quad \text{for} \quad 0 \leq |w| \leq 0.19\pi$$

$$|H(e^{jw})| \leq 0.01; \quad \text{for } 0.21\pi \leq |w| \leq \pi.$$

5) Design using impulse invariance technique and realize a Chebychev lowpass digital filter whose passband magnitude is to be within 1 dB for frequencies below 0.2π rad/sec and stopband attenuation is to be greater than 15 dB for frequencies above 0.3π rad/sec. Assume a sampling frequency of 1 Hz. (20)

6) Provide the direct-form FIR filter structures of decimator (10)

and interpolator. What are the problems in the implementation? How do you overcome these problems? Also provide the linear phase structure.

7) Explain how multirate signal processing can be used in the analysis and synthesis of speech signals in subband coding. (10)

8) Explain LMS adaptive algorithm. Explain how LMS adaptive algorithm is made use to make the Weiner Predictor Configuration adaptive based on the steepest descent technique. (10)

9) Draw the architecture of a TMS320C6X DSP processor and give the functionality of each of the block (10)

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