Question Paper

Exam Date & Time: 23-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER Master of Engineering - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2018
Monday, 23 April 2018
Time : 10:00 am to 1:00 pm

Digital Systems and VLSI Design [EDA 613]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Explain CZ method of crystal growth with relevant figures.	(10)
2)	With the relevant figures explain the different steps in raw wafer preparation.	(10)
3)	What are the uses of SiO_2 layer?	(10)
4)	Describe various photoresist performance factors.	(10)
5)	Deduce the relationship between Voltage and current in a MOSFET at different regions of operation.	(10)
6)	Explain, with neat diagrams, the following second order effects in MOSFET: a) Body Effect b) Channel-length modulation	(10)
7)	Derive an expression for the switching power dissipation component in a CMOS circuit. Discuss methods to reduce this component by analyzing each element in this expression.	(10)
8)	What is transistor sizing? What is its importance? Explain the T-sizing of the following Boolean expression: **Z = ((A.B + C) D)'**	(10)
9)	What are the various components of parasitic capacitances that show up at high frequencies? Show them in the low frequency, small signal model.	(10)
10)	How do you automate the complex logic gates layout? Explain this algorithm, with examples, which uses Euler path.	(10)

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