Question Paper

Exam Date & Time: 20-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER Master of Engineering - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2018
Friday, 20 April 2018
Time : 10:00 am to 1:00 pm
System on Chip Design [EDA 615.5]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Write short notes on Simple sequential processor and Pipelined processor	(10)
2)	Explain briefly about "Pre-Partitioning Analysis" in ESL flow	(10)
3)	Explain hardware/software co-design space	(10)
4)	What are the four design principles in SoC? Explain them briefly	(10)
5)	What are the types of branch prediction? Explain bimodal and two level adaptive predictions	(10)

6)	State the dependencies in instructions shown below. Show and describe the timing for a dataflow with three separate floating point unit and single floating point instructions. The adder unit, multiply unit and divider unit takes 2, 4 and 6 clock cycles to complete their operations respectively.
	DIV R3, R2, R1
	MUL R8, R3, R1
	ADD R4, R3, R8
		(10)

7)	What is Transaction Lookaside Buffer (TLB)? Explain the address translation with the help of a neat block diagram. Determine the average access time assuming a TLB hit ration of 0.7 with the following specification Number of entries in the TLB = 16 Time taken to conduct an associative search in the TLB = 90 ns Main memory access time = 1 us	(10)
8)	Explain the three types of cache organization	(10)

9)	Explain the criteria for choosing the suitable interconnect architecture	(10)
10)	Describe the various dimensions of the synchronization problem	(10)

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