Question Paper

Exam Date & Time: 25-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES (SOIS)
FIRST SEMESTER Master of Engineering - ME (VLSI DESIGN)
DEGREE EXAMINATION - APRIL 2018
Wednesday, 25 April 2018
Time : 10:00 am to 1:00 pm
Verification [EDA 617]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	What is Verification? Explain the need for verification.	(10)
2)	Explain the System Verilog **Logic** overcomes Verilog **reg** and **wire** construct. Explain briefly	(10)
3)	Briefly discuss the packed and unpacked array with an example and explain list of operations can be performed on arrays.	(10)
4)	Briefly discuss the dynamic and associative array with an example and explain the list of methods.	(10)
5)	Bring out the difference between Structure and union with an example.	(10)
6)	Explain in System Verilog shallow and deep copy with an example.	(10)
7)	Explain the polymorphism with an example.	(10)
8)	Explain regions of the System Verilog stratified event Queue.	(10)
9)	Briefly discuss with an example interface and virtual interface.	(10)
10)	Draw neatly and explain the SV testbench architecture.	(10)

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