Question Paper

Exam Date & Time: 18-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER ME (VLSI DESIGN)
DEGREE EXAMINATION- APRIL/MAY 2018
Wednesday, April 18, 2018
Time : 10.00 am to 1.00 pm

Advanced VLSI Design [EDA 604]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1) Discuss analog IC Design process flow with neat diagram. (10)

2) a) Discuss the gain of common source amplifier with small signal model. (10)
b) Discuss the disadvantages of single stage amplifier and suggest to overcome disadvantages.

3) Explain, with the help of a neat schematic diagram, a bandgap voltage reference. What are the advantages of this circuit over other simple references? (10)

4) What is minimum and maximum Input Common Mode Range (ICMR) of a differential amplifier? Explain with circuit diagram, how do you measure it? (10)

5) Discuss the design relationship between the compensation capacitor and load capacitor for phase margin and stability of two stage operational amplifier for negative feedback application with neat circuit diagram. (10)

6) a) Discuss single step 2-bit flash ADC architecture with neat diagram. (10)
b) Mention the disadvantages of single step Flash ADC and give the suggestion to overcome the disadvantages.

7) Discuss the disadvantages of simple resistor string DAC with diagram and discuss the design modification required to overcome the disadvantages. (10)

8) a) The n-well resistor sheet resistance is approximately 500 ohms/square (at 27 ^{o}C). The value of the total resistance (20 squares) is 10k at 27^{o}C. The temperature (10)

coefficient is 2400 ppm/^{o}C (= 0.0024). Estimate the resistance of an N-well resistor over the specified temperature ranges: 0, 10, 50 and 100 ^{o}C.
b) What are the different ways of realising the resistor design in analog IC?

9) a) Explain the channel length modulation of MOS transistors and how it is impact the analog circuit performance when the MOS transistor scaling into deep Nano meter technology node? (10)
b) Justify the proper choice of MOS transistor length (geometry size) for high speed in analog circuits without compromising gain.

10) a) If the clock frequency of parallel switched capacitor equivalent resistor is 100 kHz, find the value of the capacitor C that will emulate a 1MOhm resistor. (10)
b) Discuss the operation of switched capacitor amplifier with neat diagram

-----End-----