

# Question Paper

Exam Date & Time: 17-Apr-2018 (10:00 AM - 01:00 PM)



## MANIPAL ACADEMY OF HIGHER EDUCATION

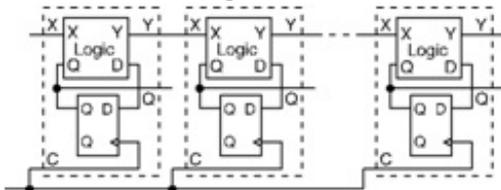
**SCHOOL OF INFORMATION SCIENCES (SOIS)**  
**FIRST SEMESTER Master of Engineering - ME (VLSI DESIGN)**  
**DEGREE EXAMINATION - APRIL 2018**  
**Tuesday, 17 April 2018**  
**Time : 10:00 am to 1:00 pm**  
**High Level Digital Design [EDA 611]**

Marks: 100

Duration: 180 mins.

### Answer all the questions.

- 1) Write short notes on the following.  
Consensus Theorem  
Significance of NAND-NAND Logic & NOR-NOR Logic (2\*5=10) (10)
- 2) Write short notes on the following with an example. (10)
  - a. With an example, explain the techniques involved in eliminating timing hazard
  - b. Priority Encoder (2\*5=10)
- 3) Design a 101 sequence detector using Moore Machine. (10)
- 4) Design the signed magnitude Comparator. (10)
- 5) Design the carry select adder & explain the benefits in variable group size. (10)
- 6) For the given circuit, Give the Min & Max Delay equation for this design. (10)



- 7) Design a dual port synchronous memory with neat diagram. (10)
- 8) Explain SLICEL in Spartan FPGA. (10)

- 9) Draw & explain the AHB design components. (10)
- 10) Design Real Time Clock with following (10)  
features.  
Display - Hr : Min : Sec  
Clock freq 200 KHz

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