Question Paper

Exam Date & Time: 20-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER ME - (VLSI DESIGN)
DEGREE EXAMINATION- APRIL/MAY 2018
Friday, April 20, 2018
Time : 10.00 am to 1.00 pm
Low Power VLSI Design [EDA 608]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Why has low power become an important issue in the present-day VLSI circuit realization?	(10)
2)	Distinguish between constant-field and constant-voltage feature size scaling. Compare their advantages and disadvantages	(10)
3)	Explain the leakage power components in detail with the help of diagrams	(10)
4)	Describe dynamic voltage scaling technique with help of block diagram	(10)
5)	A battery-operated 65nm digital CMOS device is found to consume equal amounts (P) of dynamic power and leakage power while the short-circuit power is negligible. The energy consumed by a computing task, that takes T seconds, is 2PT. Compare the below two power reduction strategies for extending the battery life: a. Clock frequency is reduced to half, keeping all other parameters constant. b. Supply voltage is reduced to half. This slows the gates down and forces the clock frequency to be lowered to half of its original (full voltage) value. Assume that leakage current is held unchanged by modifying the design of transistors.	(10)
6)	How does clock gating minimize power dissipation? Explain how it can be implemented?	(10)

7)	Explain transistor stacking and multiple threshold CMOS circuit techniques to achieve low power dissipation.	(10)
8)	Explain dynamic Vth technique with the help of a diagram	(10)
9)	Describe different types of Power Gating and its issues	(10)
10)	Explain phase assignment and algebraic transformations in the context of low power VLSI techniques	(10)

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