Question Paper

Exam Date & Time: 23-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES (SOIS)
SECOND SEMESTER ME (VLSI DESIGN)
ME DEGREE EXAMINATION - APRIL 2018
Monday, 23 April, 2018
10:00 am to 1:00 pm
Physical Design [EDA 616.8]

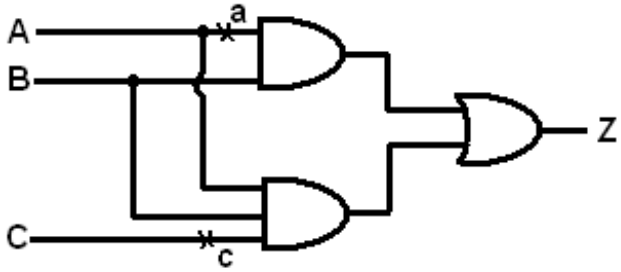
Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1) Explain the following with an example; (a) S@0 fault; (b) S@1 fault; (c) Bridge fault. (3+3+4) (10)

2) Explain the path sensitization method of test generation with an example. (10) (10)

3) For the circuit shown below in the fig. (5+5) (10)
(a) Find test vector set to detect the fault at 'c' s@1
(b) Find test vector set to detect the fault at 'a' s@0



4) Draw and explain a typical boundary scan cell. With a schematic diagram explain basic boundary scan architecture. (4+6) (10)

5) Draw and describe the detailed VLSI flow. (10)

6) What is time budget? Illustrate with an example. (10)

7) Briefly explain the following wrt to floorplan; macro placement, clock planning. (10)

8) How clock buffer/inverter insertion affects placement and timing. Explain with an example. (10)

9) Briefly discuss the detailed routing and their challenges. (10)

10) What is signoff and discuss. (10)

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