Question Paper

Exam Date & Time: 25-Apr-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER ME (VLSI DESIGN)
DEGREE EXAMINATION- APRIL
Wednesday, April 25, 2018
Time : 10:00am to 1:00pm

Universal Verification Methodology [EDA 610]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1) Explain the functionality of following components with example. (10)

Transactor (Agent)
Scoreboard

2) What is randomization? Explain the following in SystemVerilog randomization with example. (10)

Rand
Randc
Constraint block
(2+2+2+4= 10 Marks)

3) Explain the functionality of following components with example. (10)

Inheritance
Abstraction (5+5= 10 Marks)

4) Explain about uvm_component class with example. (10)

5) Write a note on UVM Integration level environment. (10)

6) Explain Clean up phase in UVM Testbench. (10)

7) Illustrate UVM Factory coding convention 1 and convention 3 with example. (10)

8) Explain different types of Object Overrides in UVM. (10)

9) Describe UVM sequences and tests with example. (10)

10) Explain different UVM reporting methods with examples. (10)

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