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MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

VI SEMESTER B.TECH. (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKE UP EXAMINATIONS, JUNE 2018

SUBJECT: EMBEDDED SYSTEM DESIGN [ELE 4001]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 20 JUNE 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.
- Support all your programs with relevant comments

1A. Classify embedded systems based on complexity. Give relevant examples. ***(03)***

1B. Write a technical note on EEMBC. List and describe in brief any five processor benchmarks developed by EEMBC. ***(03)***

1C. i. Consider the following ARM7TDMI instruction. Assume that this instruction is available at the address 0x00005020. Determine the address of the target (branching) instruction. Take the current PC content as the address of the next instruction.

0x00005020 : *B 0x7C304B*

ii. Write ARM7TDMI assembly code for the following 'C' code. Use refgisters R0 to R6 for variables 'a' to 'g' respectively.

```
if (a = = b) || ( c = = d)
{
        e = e +5;
        f = - f ;
        g = g + 4 * e;
}
```

(04)

2A. What do you mean by full ascending stack? Mention the ARM7 instructions for push and pop operation in case of full ascending stack. Illustrate with an example.. ***(03)***

2B. Write an ARM7TDMI subroutine to multiply a '32' bit unsigned number by 72. Do not use any instruction for multiplication. Assume the number to be passed to subroutine through 'R0' register. Return the result through 'R1' register. If the number is greater than 0x0000F000, return back without multiplication with 01 as error code in 'R2' register. ***(03)***

2C. Describe the following ARM7TDMI exceptions.

i. Prefetch abort
ii. IRQ interrupt

(04)

3A. Describe the operation performed by ARM7TDMI in the three stages of instruction execution and hence explain the three stage pipeline architecture. Illustrate with an example, pipeline flush necessary in case of branching instructions. ***(04)***

3B. With the help of relevant diagram, explain the strobe protocol with respect to

i. Read operation
ii. Write operation. ***(03)***

3C. Explain the hardware bus arbitration scheme used by PCI parallel communication bus to support multi master configuration.

Describe the role of FRAME and DEVSEL signals during PCI bus transactions. ***(03)***

4A. i. Describe the Least Recently Used replacement policy with respect to cache memory. What are the merits and demerits of this scheme?

ii. In a system with two levels of cache, out of 1600 memory references, there are 100 misses in L1 cache and 45 misses in L2 cache. L1 access time is 3clock cycles, L2 access time is 12 clock cycles and main memory access time is 100 clock cycles, determine the average memory access time. What will be the average access time if L2 cache is not included in the system (only L1 cache present). ***(04)***

4B. Write a 'C' program for PIC16f877 microcontroller to configure the MSSP in I2C master mode to transmit data bytes AAH and BBH to slave device '1' with address 3AH and then (before stop condition is issued) transmit data bytes 55H and 66H to slave device '2' with address 48H at 400kbps baud rate. Assume fosc = 16MHZ. ***(03)***

4C. Explain the following with respect to USB serial communication bus.

i. Supported data transfer rates(bandwidth)
ii. Control and Bulk (data) transfer. ***(03)***

5A. i. Describe the salient features of IRDA Wireless communication protocol; list the various standards and data transfer rates supported by IRDA.

ii. With the help of a relevant diagram, describe the functions of IR encoder / decoder and IR transceiver in realizing SIR communication. ***(04)***

5B. With the help of a relevant diagram, describe daisy chain arbitration scheme of interrupt expansion. List the merits and demerits of this scheme by comparing it with priority arbitration scheme. ***(03)***

5C. List the various metrics to be optimized while designing an embedded system and describe the Time to Market design metric in detail. ***(03)***