Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION - APRIL- 2018

SUBJECT: ELECTRONIC SYSTEM DESIGN (ECE - 4023)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss in detail the different stages of electronic system development. Why do we need reverse engineering?

1B. Draw neat Ishikawa diagram for failure of fiat cars in India and suggest solutions for this issue.

1C. Discuss Kolb's Experiential learning theory with a neat diagram.

(5+3+2)

2A. Explain any two fundamental noise mechanisms and draw the noise model for any two circuit elements with relevant equations.

2B. Realize resonance based micro cantilever chemical sensor for the following specifications: L=200µm, t=4µm, w=10µm. Assume density of polysilicon =2200 kg/m^3 and E= 1.78x10^{11} P_a . Find resonance frequency of the beam. The above beam is used for detection of CO_2 level present in your class room. The least count of frequency measurement is 2 kHz. Find the mass sensitivity of cantilever and prove that micro cantilever chemical sensors measure microgram of target chemicals.

2C. What is the role of the quality assurance section in an electronic product development?

(5+3+2)

3A. Explain any two commonly used heat transfer mechanisms in electronic system design.

3B. Write the features and drawbacks of Surface Mount Devices.

3C. A power transistor has a thermal resistance of 200^o C/W.

i) Calculate the maximum permissible power dissipation, when the T_{Jmax}=90^{o}C and T_A=25^{o}C.

ii) If the heat sink is used and thermal resistance is reduced to 100^{o}C/W, calculate the maximum permissible power dissipation.

(5+3+2)

4A. With neat flow diagram explain the major steps involved in the production of a double-sided, plated through-hole Printed Circuit Board.

4B. Given that V_{ref} = 5V and C = 0.1pF design a 3 bit charge scaling DAC. Find the value of the output voltage for $D_2D_1D_0$= 011.

4C. A circuit consists of 200 components with failure rate of 10x10^{-9} / hr and 400 hold joints with failure rate 100x10^{-9} /hr. Calculate Mean Time Between Failure for this circuit.

(5+3+2)

5A. Draw and explain the melting point diagram of tin and lead alloys in the soldering techniques. Why does the electronic industry employ 60/40 solder.

5B. Explain the working of the typical circuit of switched mode power supply with neat diagram. Compare its merits and demerits with other power supplies.

5C. With help of a suitable example, elaborate the points to be considered while selecting a touch screen.

(5+3+2)