Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
APRIL 2018
SUBJECT: EMBEDDED SYSTEM DESIGN (ECE -4003)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw and explain the simplified revenue model for computing revenue loss from delayed entry. Obtain the equation for percentage revenue loss and compute the percentage revenue loss if D=5 and W=10. If the company whose product entered the market on time earned a total revenue of $25 million, how much revenue did the company earned that entered market 5 months late.

1B. List and define the three main processor technologies. What are the benefits of using each of the three different processor technologies?

1C. Define following metrics of system design

i. NRE cost ii. Time-to-prototype iii. Market window iv. Maintainability

(5+3+2)

2A. With what aspects are the following different.

(a) RISC and CISC architecture
(b) Harvard and Von-Neuman architecture.
(c) Big Endian and Little Endian addressing.
(d) COTS and ASICS
(e) SRAM and DRAM

2B. What is Brown out protection circuit? With neat circuit diagram, explain its working.

2C. Write the different stepping modes of bipolar stepper motor and give the table for the same.

(5+3+2)

3A. Explain I2C and SPI communication interfaces with neat diagrams.

3B. Represent and explain possible states and state transitions of the processes of an Operating system with the help of state machine diagram.

3C. Explain the following terms of OS scheduling

i. Priority Inheritance
ii. Priority ceiling

(5+3+2)

4A. Three processes with process ID's P1, P2, P3 with estimated time 7,9,3 milliseconds respectively enters the ready queue together. Process P4 with estimated execution completion time 4ms enters the ready queue after 1ms. Process P5 with estimated execution time 10ms enters the ready queue after 6ms. Calculate the waiting time and TAT for each processes. Also calculate average waiting time and average TAT in the non-pre-emptive SJF scheduling. What are the drawbacks of SJF scheduling?

4B. Design an automatic tea/coffee vending machine based on FSM model for the following requirement.

The tea/coffee vending is initiated by user inserting a 5 rupee coin. After inserting the coin, the user can either select ‘Coffee’ or ‘Tea’ or press ‘Cancel’ to cancel the order and take back the coin.

4C. Write an embedded C program using a super loop to count the number of 0’s received in port1 of 8051 and display the count on port2 of 8051.

(5+3+2)

5A. What is EDLC? With a neat diagram explain the different phases of EDLC.

5B. Explain two commonly used firmware embedding techniques for a non-OS based embedded system

5C. Explain the following storage classes used in embedded system

a) NEAR b) XDATA c) BIT d) CODE

(5+3+2)