Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATIONS, JUNE - 2018

SUBJECT: DIGITAL SYSTEM DESIGN [ICE 4001]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. What are fixed function IC's? Where are they used? What are its disadvantages?

1B. What are the different operators used in VHDL? Give examples for each.

1C. Implement the following Boolean Function using PAL with 4 Inputs and 3 Wide AND-OR structure. Also write the PAL programming table.

$F1(A,B,C,D) = \sum m(2,12,13)$

$F2(A,B,C,D) = \sum m(7,8,9,10,11,12,13,14,15)$

$F3(A,B,C,D) = \sum m(0,2,3,4,5,6,7,8,10,11,15)$

$F4(A,B,C,D) = \sum m(1,2,8,12,13)$

(2+3+5)

2A. Explain When Else signal assignment using an example.

2B. Write a note on ROM Organization with a block diagram.

2C. Design a sequence detector circuit to detect the sequence 1101 using a Moore Machine. Write a structural code assuming suitable components.

(2+3+5)

3A. Draw a neat Y Chart showing the different levels and domains.

3B. With a neat timing diagram, write a VHDL Code for a divide by 4, divide by 8 clock divider. Assume a negative edge triggered DFF for circuit implementation with active high reset that operates on a 60MHz clock frequency.

(4+6)

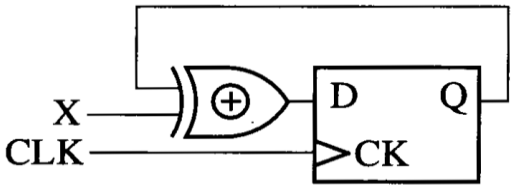
4A. Draw a block diagram for a Mealy Machine and write a generic Behavioural code.

4B. Write a test bench to verify the working of a 4 bit binary adder.

(5+5)

5A. What are some of the sequential statements in VHDL? Explain one with an example.

5B. In the circuit shown below, the D flip-flop has a setup time of 4 ns, a hold time of 2 ns, and a propagation delay from the rising edge of the clock to the change in flip-flop output in the range of 6 to 12 ns. The XOR gate delay is in the range of 1 to 8 ns.
What is the minimum clock period for proper operation of the network?
What is the earliest time after the rising clock edge that X is allowed to change?



5C. With neat figures discuss various types of interconnects in FPGAs.

(2+3+5)

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