Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SIXTH SEMESTER B.Tech. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER DEGREE EXAMINATION APRIL - 2018

SUBJECT: DIGITAL SYSTEM DESIGN [ICE – 4001]

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. What is system level synthesis?

1B. Design a ROM that accepts a 3-bit number and generates an o/p binary number equal to the square of the input number.

1C. Mention various steps to design a combinational circuit. Design a 4:1 Mux using logic gates and write a structural VHDL code for the same assuming suitable components.

(2+3+5)

2A. What are the differences between Mealy and Moore Machine?

2B. Show how a PLA can be used to implement a full adder.

2C. Design a sequence detector circuit to detect the sequence 1110 using a Mealy Machine. Write a behavioural code for the same.

(2+3+5)

3A. Draw a block diagram of a Moore Machine.

3B. What are case statements? Explain with an example.

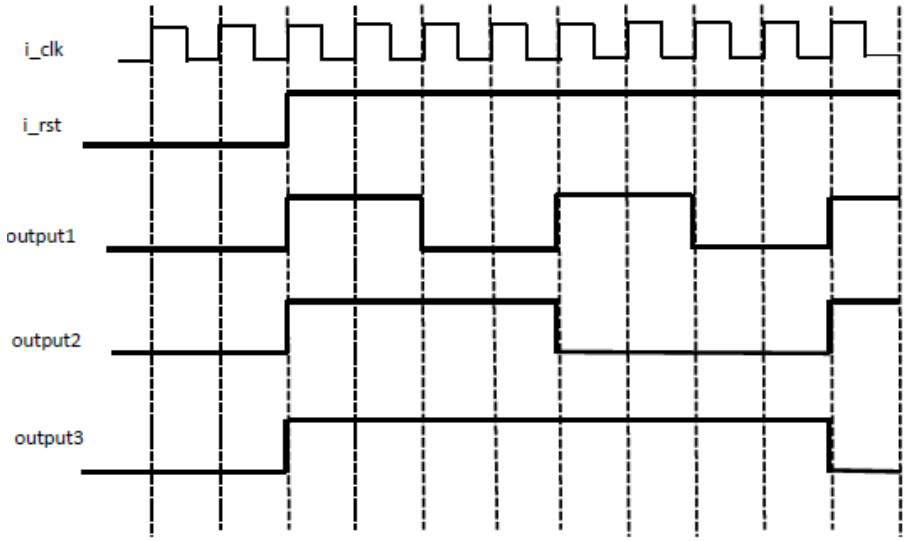
3C. Draw a neat Y Chart and describe how electronic systems are separated into different domains and described along different levels.

(2+3+5)

4A. Write syntax for a Process statement. What does the sensitivity list signify?

4B. Write a test bench for a positive edge triggered D FF. Consider the clock frequency to be 3 MHz and active low reset.

4C. For the timing diagram shown in the figure, write a VHDL code using concurrent signal assignment for signal generation.



(2+3+5)

5A. Draw a neat timing diagram showing setup time, propagation delay and hold time for a D Flip Flop.

5B. Write a note on SRAM Programming Technology.

5C. With neat figures discuss various types of FPGA Architecture.

(2+3+5)

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