Question Paper

Exam Date & Time: 26-Nov-2018 (08:30 AM - 11:30 AM)

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

FIRST SEMESTER B.TECH END SEMESTER EXAMINATIONS, NOV 2018

Basic Electronics [ECE 1051 - 2018 -PHY]

Marks: 50 **Duration: 180 mins.**

A

Answer all the questions.

Instructions to Candidates: Answer ALL questions Missing data may be suitably assumed

1) A) For the biasing circuit shown in figure Q1A with silicon transistor, $R_1 = 39k\Omega$, $R_2 = 8.2k\Omega$, $R_C = 3.3k\Omega$, $R_E = 1k\Omega$, $V_{CC} = 18V$, $V_{BE} = 0.7V$ and $\beta = 120$. Determine I_B, I_C, V_{CE}, V_E and V_B. (4)

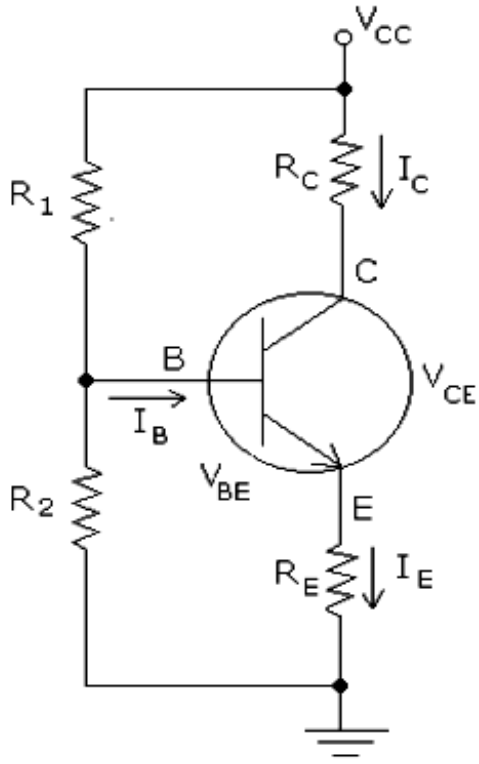

Figure Q1A

B) Draw the circuit diagram of a full wave bridge rectifier with capacitor filter. Given $V_m = 24V$, $R_L = 1k\Omega$, $C = 1000\mu F$ and $f = 50Hz$, calculate the DC voltage and ripple factor. (3)

C) Draw the circuit diagram of RC coupled amplifier and discuss the role of coupling capacitor and emitter bypass capacitor. (3)

2) A) (i) Draw the circuit diagram of an OPAMP non inverting amplifier and derive the expression for its output voltage. (4)

(ii) The inputs to the OPAMP are $V_{1(non\text{-}inv)}$ = 3.5mV and $V_{2(inv)}$ = -1.5mV. If the differential gain is 60dB and CMRR is 40dB, calculate the output voltage.

B) In an OPAMP comparator circuit V_{ref}=-2V is applied to the non-inverting terminal and V_{in}=10sin(ωt) V is applied to the inverting terminal. Draw the circuit diagram and plot the input and output waveforms. Assume V_{sat} = ±15V. (3)

C) Subtract $(11.75)_{10}$ from $(5.50)_8$ using 2's complement method. (3)

3) A) In a certain application, four inputs A, B, C, D are fed to a logic circuit, producing an output Z which controls a relay. Z = 1 for the input states (ABCD): 0000, 0010, 0101, 0110, 1101 and 1110. The states 1000 and 1001 do not occur and Z = 0 for the remaining input states. (4)

i) Obtain truth table for Z.

ii) Use Karnaugh map to find a minimal SOP and implement the same using NAND gates only.

B) Draw the logic circuit of 3 bit up counter using negative edge triggered JK flip-flops. Also sketch the timing diagram. (3)

C) With a neat logic diagram and table explain the shifting of data 111011 in a Serial-In Serial-Out 4-bit shift register. Also mention how many clock cycles are required to shift the MSB of above mentioned data to the output. (3)

4) A) Define frequency modulation. Sketch frequency modulated signal in time domain for a sinusoidal modulating signal. A carrier of peak amplitude 5V and frequency 90MHz is frequency modulated by a sinusoidal voltage of peak amplitude 5V and frequency 10 KHz. If the frequency sensitivity is 10Hz/V, calculate the frequency deviation and modulation index. Write the equation for the resulting FM wave. (4)

B) The output current of a 60% modulated AM signal generator is 1.5A. To what value will this current rise if the generator is modulated additionally by another audio wave, whose modulation index is 0.7? (3)

C) Highlight three important reasons why modulation is required in wireless communication. (3)

5) List the different types of analog pulse modulation schemes. Describe each with relevant waveforms. (4)

A)

B) Sketch the modulated signal waveforms for ASK, FSK and PSK if the modulating data stream is 10101. (3)

C) Explain the following terms with reference to electronic communication systems (3)

i) TDMA ii) MAN iii) EIR

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