Question Paper

Exam Date & Time: 01-Dec-2018 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLED SCIENCES
II SEMESTER B.S. ENGINEERING END SEMESTER EXAMINATION- NOVEMBER/DECEMBER 2018
Computer Organization and Architecture [ICS 122]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.
Missing data, if any, may be suitably assumed

1) Explain the characteristics of RISC and CISC Instruction set. (4)

A)

B) Give the signed magnitude, 1's complement and 2's complement representation of the following decimal numbers. (6)
i) -7
ii) +7

C) Explain the following addressing modes by giving an example for each. (10)
i) Index
ii) Immediate
iii) Absolute
iv) Register
v) Indirect

2) What is sign extension? Explain with an example for both positive and negative numbers. (4)

A)

B) Given A=7 (multiplicand) and B=3 (multiplier), compute the product using Booth's algorithm. Clearly show all the steps. (8)

C) Write the block diagram of hardware for addition and subtraction and explain the same. (8)

3) Divide 6 by 2 using restoring division technique. Clearly indicate all the steps. (8)

A)

B) Write the Add Rule and Multiply rule used for adding and (8)

multiplying 2 floating point numbers.

	C)	Give the format of IEEE 32 bit floating point representation, Convert 34.625 to binary and represent in IEEE 32 bit floating point representation.	(4)
4)	A)	With a neat diagram, explain the Data Flow in the Fetch cycle of the processor.	(6)
	B)	Give the sequence of microinstructions for the execute cycle of ADD R1,X instruction which adds the contents of location X to Register 1 and puts the result in R1	(6)
	C)	Draw the block diagram of the control unit showing all of its input and output and explain the same.	(8)
5)	A)	With a neat diagram, explain the operation of a static RAM cell	(6)
	B)	Explain the structure of an optical disc with the help of a diagram and discuss how information is read from and written onto the disc.	(8)
	C)	A computer has a small data cache capable of holding four words. Each cache block consists of one word. When a given program is executed, the processor reads data sequentially from the following addresses: A, B, C, A, D, E, A, D, C, F (i) Assume that the cache is initially empty. Show the contents of the cache for LRU replacement algorithm and compute the hit rate. (ii) Repeat part (i) for the cache that uses the FIFO replacement algorithm and compute the hit rate. Indicate clearly all the steps.	(6)
6)	A)	Explain Direct mapping and Associative mapping used to map main memory to cache memory, with the help of an example for each.	(6)
	B)	Draw the structure of a 4K X 8 memory using 1K X 4 memory chips. Indicate clearly, the number of address lines and the data lines in the diagram.	(6)
	C)	With a neat timing diagram, explain the input transfer on synchronous bus.	(8)
7)		What is an interrupt? What is enabling and disabling of	(8)

A) interrupts? Explain the sequence of events involved in handling an interrupt request from a single device.

B) With a neat block diagram, explain the operation of a parallel output interface. (8)

C) Write a note on ring based Interconnection networks (4)

8) Explain the 2 state algorithm used for dynamic branch prediction. (4)

A)

B) What is data hazard? Explain how data dependencies are handled (8)
i) using operand forwarding
ii) in software

C) Explain how cache coherence problem in a shared multiprocessor system is addressed when Write-through protocol is used. (8)

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