Question Paper

Exam Date & Time: 14-Nov-2018 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
THIRD SEMESTER B.Sc. Applied Sciences in Engg.
END-SEMESTER THEORY EXAMINATIONS NOVEMBER - 2018
ANALOG ELECTRONIC CIRCUITS [IEC 231]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) Draw the circuit diagram of common emitter configuration using NPN transistor. Draw and explain the input and output characteristics. Indicate cut-off, saturation and active regions. (5)

B) In a certain transistor, the emitter current is 1.02 times as large as the collector current. If the dc emitter current is 12 mA, the reverse saturation current I_{CO} is $20\mu A$, determine the common base and common emitter reverse saturation currents, the base current, α_{dc} and β_{dc}. (5)

C) Draw the small signal equivalent of the CE amplifier shown in Fig Q1C. Define the small signal parameters. Obtain the expressions for the voltage gain, input resistance and output resistance of the amplifier from the model. (5)

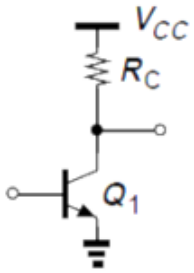


Fig Q1C

D) (5)

For the transistor circuit shown in **fig Q1D**, $R_{in} = 92K\Omega, R_L = 820\Omega$ and $V_{CC} = 10V$. With the help of above data and values given in **Table Q1D**, Determine V_{BE} , V_{CE} and the region of operation. Show all necessary steps. Explain briefly the working of the circuit and draw the output waveform.

Table Q1D

V_{in}	I_B	I_C	V_{BE}	$V_{CE}(V_{out})$	Operating Region
10V	112μA	12mA	?	?	?
0V	0	?	?	?	?

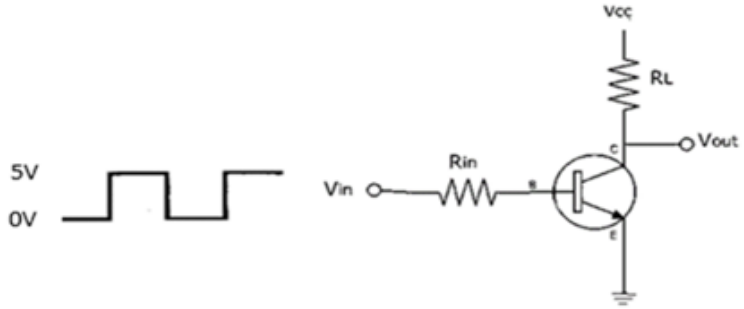
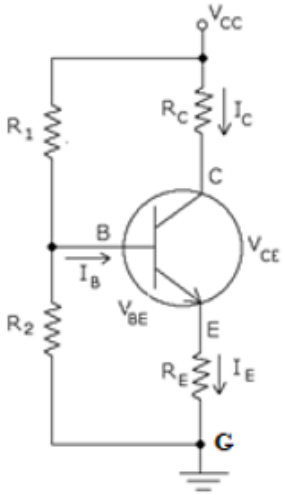


Fig Q1D

2) A) Determine I_B, I_C, I_E, V_{CE}, V_B, V_C and V_E for the voltage divider configuration shown in **Fig Q2A** given that V_{CC}=12V, R_1=39kΩ, R_2=8.2kΩ, R_C= 3.3kΩ, R_E=1 kΩ and β=120.Assume V_{BE}=0.7V. What is the region of operation? Neglect I_{CO}. (10)



FigQ2A

B) Draw the circuit diagram of RC coupled amplifier without feedback using NPN transistor. Mention the function of each component. Explain the working at low, medium and high frequencies. (5)

C) Draw and explain the frequency response of RC coupled amplifier with and without feedback. (5)
In a 3-stage RC coupled amplifier, if the individual stage voltage gains are: $A_1 = 20dB, A_2 = -7dB$ and $A_3 = 5dB$ respectively, find the output voltage at each stage and overall gain in decibels if the input voltage applied is $V_i = 10\sin(2\pi ft)$ millivolts.

3) (5)

A) For the circuit in **Fig. Q3A**, $\mu_n C_{ox} = 200\ \mu A/V^2$ and $V_{TH} = 0.5V$. Calculate

i) Drain current.

ii) If the gate voltage increases by 10 mV, what is the change in the drain voltage?

iii) What choice of R_D places the transistor at the edge of the triode region with value of I_D as in part i)?

iv) Determine the value of W/L that places M_1 at the edge of saturation with V_{GS} as in part i).

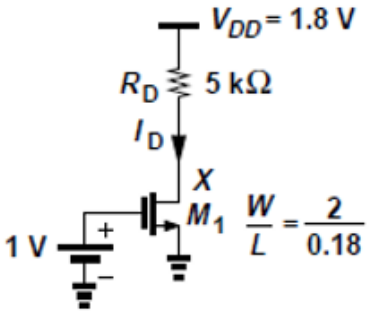


Fig Q3A

B) (5)

Calculate the maximum allowable gate voltage in **Fig. Q3B**, if M_1 must remain saturated. Assume $\mu_n C_{ox} = 200\ \mu A/V^2$ and $V_{TH} = 0.5V$

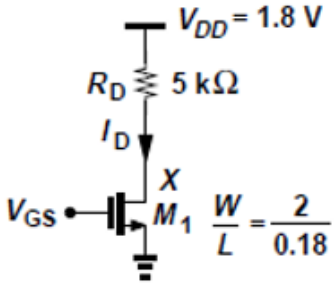


Fig Q3B

C) (5)

If λ= 0.1 / V and $W/L = 20/0.18$, construct the small-signal model of the circuit shown in **Fig. Q3C.** Compute g_m and r_o

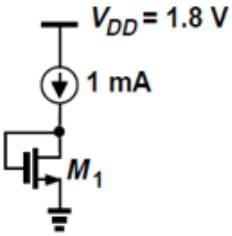


Fig Q3C

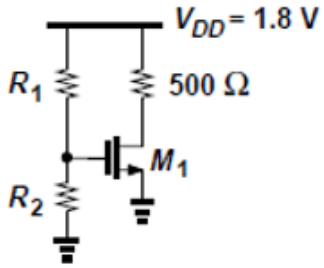
D) (5)

An NMOS device with $\lambda = 0.2/V$ must provide a gain of 20 with V_{DS} = 1.5 V. Determine the required value of W/L, if I_D = 0.5 mA.

4) (5)

A)

Design a circuit of **Fig. Q4A** for a drain current of 1 mA. if $^{W}/_{L} = {}^{20}/_{0.18}$, $V_{TH} = 0.5V$, Compute R1 and R2 such that the input impedance is at least 30 k.Ω



FigQ4A

B) (5)

If $^{W}/_{L} = {}^{10}/_{0.18}$, $\mu_p C_{ox}$ = 100 μA/V² and λ= 0, determine V_{GS}, V_{DS} and I_D for the circuit shown in **Fig. Q4B**. Draw the small signal model.

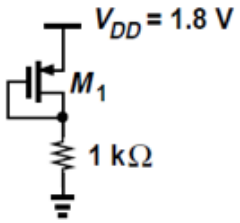


Fig Q4B

C) (5)

The CS stage of **Fig. Q4C** must provide a voltage gain of 10 with a bias current of 0.5 mA. Assume $\lambda_1 = {}^{0.1}/_{V}$, and $\lambda_2 = {}^{0.15}/_{V}$.

(a) Compute the required value of $(^{W}/_{L})1$.

(b) If $(^{W}/_{L})2 = {}^{20}/_{0.18}$, calculate the required value of V_b.

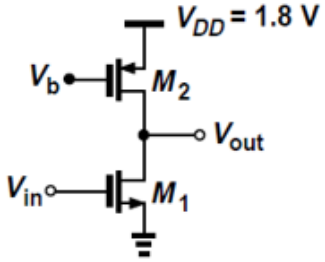


Fig Q4C

D) (5)

In the circuit of **Fig. Q4D**, M_1 and M_2 have lengths equal to 0.25 µm, $\mu_n C_{ox}$ = 200 µA/V^2 , V_{TH} = 0.5V,and $\lambda = {}^{0.1}/_{V}$. Determine W_1 and W_2 such that $I_X = 2I_Y = 1$ mA. Assume $V_{DS1} = V_{DS2} = V_B = 0.8$V. What is the output resistance of each current source?

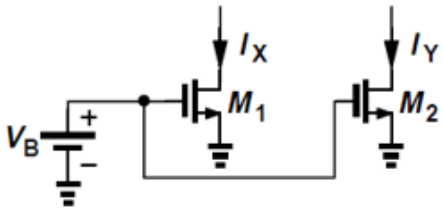


Fig Q4D

5) A) Draw the circuit diagram of a Colpitts oscillator. If C_1=100 pF, C_2=7500 pF and the inductance is variable, determine the range of inductance values, if the frequency of oscillation is to vary between 950 KHz and 2050 KHz. (5)

B) State and prove Miller's theorem. For the circuit shown in **Fig Q5B**, draw the small signal model. Using Miller's theorem, determine Miller's input and output impedances. (5)

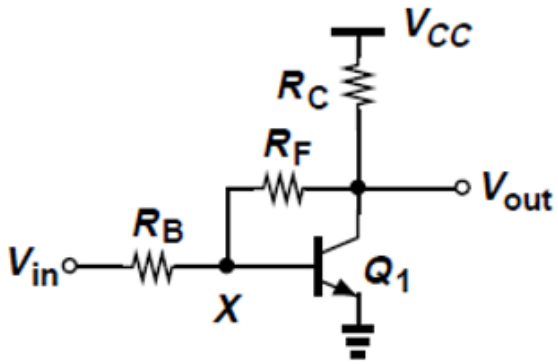


Fig Q5B

C) Draw the circuit diagram of a Transformer coupled Class B push pull amplifier and write the expression for power efficiency. What is crossover distortion in class B amplifier and how is it overcome? (5)

D) Using block schematic of a voltage series feedback amplifier, derive expressions for voltage gainA_V, input resistance R_{if} and output resistanceR_{0f}. Determine the values of A_{Vf}, R_{if} and R_{of} if A_V =-50, R_i=50k and R_o= 1k. (5)

6) A) It is desired to design a phase shift oscillator using an FET having g_m=5000µmhos, r_d=40kΩ and feedback circuit resistor R=10KΩ, determine the value of capacitor for oscillator operation at 1 KHz and also determine the R_D for A_V>29 to ensure oscillator action. Draw the circuit diagram. (5)

B) Draw the self-bias circuit of a CS amplifier. Construct the high frequency model and obtain the expressions for cutoff frequencies. (5)

C) (5)

An amplifier with negative feedback gives an output of 12.5V with an input of 1.5V. When feedback is removed, it requires 0.25 V input for the same output. Find a) value of voltage gain without feedback b) value of feedback factor β.

D) Design a passive RC low pass filter with a cutoff frequency of 500Hz using a 220pF capacitor. Draw the circuit diagram and plot the frequency response. What is the output at the cutoff frequency? (5)

7) A) Draw the block schematic of i) Voltage shunt ii) Current series feedback amplifiers. What is the effect of series and shunt feedback on the input and output resistance of an amplifier? (5)

B) Define class A, class B and class AB power amplifiers. With the help of output characteristics and the dc load line, illustrate their operation. What are the theoretical efficiencies of a series-fed class A and class B power amplifiers? (5)

C) Draw the circuit diagram of a crystal oscillator and explain the working. Mention any two advantages of Crystal oscillators. (5)

D) Draw the circuit diagram of a self-bias CS stage amplifier with coupling and bypass capacitors. Write the expression for voltage gain and explain with relevant expressions, how the lower cutoff frequency is chosen? (5)

8) Explain the following: (4X5) (20)

i) Early effect in BJT
ii) Channel length modulation in MOSFET
iii) Positive and Negative feedback
iv) Barkhausen Criterion for oscillation

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