# Question Paper

Exam Date & Time: 22-Nov-2018 (02:00 PM - 05:00 PM)

## MANIPAL ACADEMY OF HIGHER EDUCATION

### INTERNATIONAL CENTRE FOR APPLIED SCIENCES
### THIRD SEMESTER B.SC. Applied Sciences in Engg.
### END - SEMESTER THEORY EXAMINATIONS NOVEMBER - 2018
### ANALOG AND DIGITAL SYSTEM DESIGN [IMET 234 - S2]

**Marks: 100** **Duration: 180 mins.**

**Answer 5 out of 8 questions.**

**Missing data, if any, may be suitably assumed**

1) A) Design 4-bit parallel adder cum subtractor using single 74LS283 IC and additional gates (6)

B) Implement function f(A,B,C)=$\sum$ m (1,4,6,7) using (i) 8:1 Mux (ii) 4:1 Mux (iii) 2:1 Mux (10)

C) Draw the circuit diagram & output waveform for precision Full wave rectifier (4)

2) A) Design a 4-bit BCD to Excess-3 code converter (10)

B) Explain the operation of Astable multivibrator using 555 timer with the help of internal circuit diagram and also derive the design equations for time period and duty cycle (10)

3) A) What is a priority encoder? How is it different from encoder? Design a 8:3 priority encoder and explain its operation (10)

B) Explain the operation of Mono-stable multivibrator using OP-AMP with the help of circuit diagram and also derive the design equation for pulse time period. (10)

4) A) Design a combinational logic circuit that will detect various inputs conditions for 4 inputs (DCBA). The circuit will generate the following outputs:
- Output GT will be HIGH if the input value is greater than 9.
- Output LT will be LOW if the input value is less than 4.
- Output RNG will be HIGH if the input is greater than 6 and (10)

less than 11.
- Output signal TEN will be LOW if the input is equal to 10.
The design should include; Truth Table, K-Maps, and Logic equations.

B) Explain the operation of 4-bit SAR type ADC with the help of relevant diagrams and also mention the advantages and disadvantages of SAR type ADC compared to Flash type ADC (10)

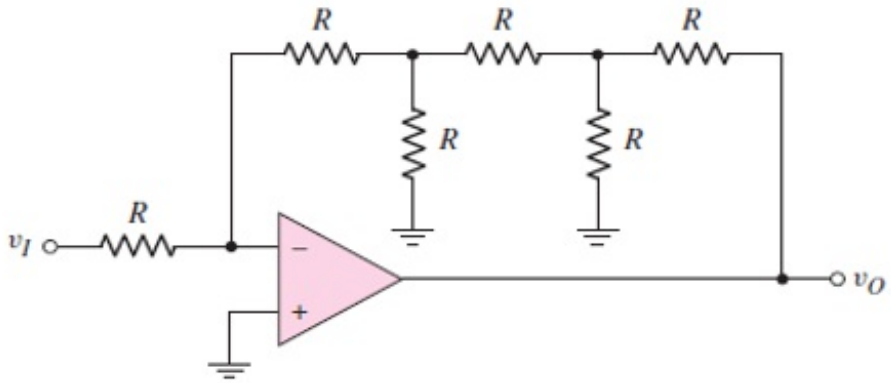
5) A) Design a 4-bit BCD to EXCESS3 adder with the help of 74LS283 parallel adder IC and additional gates if required. Hence add 6 to 8 using above design (10)

B) Design a timer using 555 IC to generate frequency of 1kHz at 50% duty cycle. Connect one RED LED & one GREEN LED so that for 0.5ms the RED LED is ON and GREEN is OFF and for the next 0.5ms the GREEN LED is ON and RED if OFF. LEDs power supply rating is 5V and 50mA. (10)

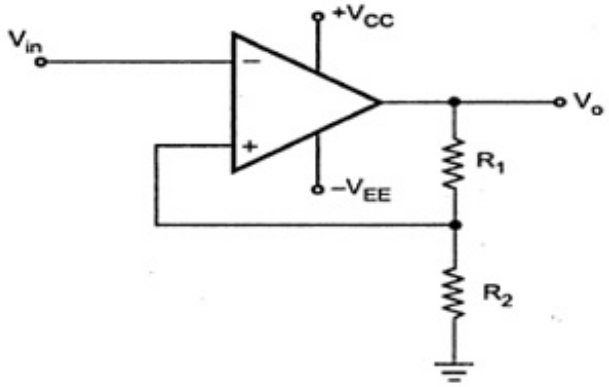
6) Convert SR flip-flop to JK Flip flop (8)

A)

B) Find gain in the circuit shown below Fig., if all resistances are equal. (8)




C) For the circuit shown in Fig., calculate the values of R1 and R2 if saturation voltages are +12 V and -12V. Assume hysteresis width = 6V (4)




7) Design a synchronous DECADE up counter using J-K flip flop (10)

A)

B) Draw the block diagram of PLL and explain its operation. (5)

C) Explain the operation of D Flip-flop with the help of Logic diagram also derive Characteristic equation from Characteristic table. (5)

8) Design a 4-bit universal shift register to operate in the following modes: (10)

A)

| Mode control | | Operation |
|---|---|---|
| S0 | S1 | |
| 0 | 0 | No change |
| 0 | 1 | Shift right |
| 1 | 0 | Shift left |
| 1 | 1 | Parallel load |

B) Using IC 7805(Three terminal regulator), design a current source to deliver 0.15Amp current to 20Ω, 5 watt load (10)

[quiescent current = 4.2mA for 7805 IC]. What is the minimum input voltage required to the regulator? What is the output voltage?

Also draw the LM 317 protective circuit

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