Question Paper

Exam Date & Time: 20-Nov-2018 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
THIRD SEMESTER B.SC. Applied Sciences in Engg.
END - SEMESTER THEORY EXAMINATIONS NOVEMBER - 2018
COMBINATIONAL AND SEQUENTIAL LOGIC [EC 231]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data, if any, may be suitably assumed

1) A)
(i) Add 548.6 + 280.37 in BCD number system (6)
(ii) Convert the following to the indicated bases $(34F.B)_{16}$ = (?) $_8$ $(84.3)_{10}$ = (?)$_2$
(iii) In an odd parity scheme which of the following contains an error
(a) $(10110111)_2$ (b) $(11101010)_2$

B) Design a combinational circuit to detect the decimal numbers 0,1,3,5 and 7 in a BCD input. (4)

C) Simplify the following function using karnaugh map and draw the circuit for the simplified expression using NAND gates. Also determine the essential prime implicant $F(A,B,C,D)=\sum m(0,4,5,10,11,13,15)$ (5)

D) Write a dataflow VHDL code for 8 to 3 encoder (5)

2) A)
Simplify the following Boolean expression (5)
(a) AB+(AC)'+AB'C(AB+C) (b)[A+(BC)']'(AB'+ABC)

B) Design a combinational circuit to convert BCD to gray code using basic gates. (5)

C) Using Quine Mccluskey method, Obtain the minimal sum for (10)

$F(A,B,C,D)=\sum m(0,1,6,7,8,9,13,14,15)$

3)	A)	With a neat circuit diagram, explain the working of 4 bit binary adder/subtractor	(5)
	B)	Implement the following function $F(A,B,C,D) = \sum m(0,1,3,4,8.9,15)$ using (i) 8:1 multiplexer and basic gates (ii) 4:1 multiplexer and basic gates	(5)
	C)	Implement the following multiple output combinational circuit using 4 to 16 decoder with active low outputs. $F1=\sum m(0,1,2,6)$ $F2=\sum m(2,4,6)$ $F3=\sum m(0,1,5,6)$ $F4=\sum m(0,1,4,7,12,14,15)$	(5)
	D)	Write a behavioral VHDL code for 8:1 multiplexer using case statement	(5)
4)		Implement the function $F=\sum m(0,2,4,6,7,8,10,12,13,15)$	(5)
	A)	using PLA.	
	B)	Design a circuit for 4 to 2 priority encoder using basic gates	(5)
	C)	Convert (i) JK flipflop to SR flipflop, (ii) SR flipflop to T flipflop	(5)
	D)	Design a Mod 6 ripple up counter using T flipflop	(5)
5)	A)	Design a synchronous counter that goes through states 0,1,2,4,0,....The unused states must always go to zero (000) on the next clock pulse	(10)
	B)	Explain the operation of a master slave JK flipflop with a neat circuit diagram	(5)
	C)	Draw the logic diagram of gated SR latch using NAND gates. Derive the truth table for the same and explain its operation	(5)
6)	A)	With a neat circuit diagram, explain the operation of 4 bit Universal Shift register for the following table	(10)

S_1	S_0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

B) Reduce the following state table and draw reduced state diagram (5)

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

C) Write the behavioral VHDL code for 4 bit parallel in serial out shift register (5)

7) A) Analyze the following synchronous sequential circuit. Draw the logic circuit, excitation table / state table and state diagram, X is the input, A&B are the outputs. (10)

$J_A=B$, $J_B=X'$, $K_A=X'B$, $K_B=A$ xor X

B) Design a Mealy type Sequence detector to detect an overlapping sequence "1010" (10)

8) A) Write the structural VHDL code for 8:1 multiplexer using 2:1 multiplexer (Code needs to be written for entire hierarchy). (10)

B) Explain the operation of 4 bit Ring counter with a neat circuit diagram and suitable timing waveforms. (5)

C) Define the following terms with an example (5)
(i) Self complementing code.
(ii) Unit distance code.

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