Question Paper

Exam Date & Time: 20-Nov-2018 (02:00 PM - 05:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTER FOR APPLIED SCIENCES
END SEMESTER EXAMINATION NOV./DEC. 2018
SWITCHING CIRCUITS AND LOGIC DESIGN [ICS 232]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.
Missing data may be suitably assumed

1) A) i) Express DeMorgan's theorem in terms of logic gates. **4M** (8)

ii) Draw the NAND gate and NOR gate realization of f (x1, x2, x3) = $\sum$m(2, 3, 4, 6, 7). **4M**

B) Simplify the following expressions using algebraic manipulation. (12)

i) f= (x1+x3+x4).(x1+x2'+x3).(x1+x2'+x3'+x4) **3M**

ii) A'B+A'B'C'D'+ABCD' **3M**

iii) f= (x1+x2+x3).(x1+x2'+x3).(x1'+x2'+x3).(x1+x2+x3') **3M**

iv) f= x1x2'x3'+x1x2x4+x1x2'x3x4' **3M**

2) A) i) Define the terms implicant, prime implicant, essential prime implicant and cover. **4M** (10)

ii) Consider the function f(x1, x2, x3, x4) = $\sum$m(0, 2, 4, 5, 10, 11, 13, 15). Using k-map, find the prime implicants, essential prime implicants and minimal cover. **6M**

B) i) Using k-map, determine the simplest SOP and POS expressions for the function f (x1, x2, x3, x4) = $\sum$m(4, 6, 8, 10, 11, 12, 15) + D(3, 5, 7, 9). **6M** (10)

ii) Consider the function f(a,b,c,d)= $\sum$m(0, 4, 5, 6, 9, 10, 11, 15). Use functional decomposition to find the minimal SOP expression for f. **4M**

3) A) Consider the function F(w,x,y,z)= $\sum$(1,4,6,7,8,9,10,11,15). Using tabulation method, find the minimal SOP expression (10)

for F.

B) Represent the following pairs of decimal numbers using 6-bit 2's-complement system, then subtract the second number from the first using binary addition. State whether or not overflow occurs in each case. (10)
a) +22 and +31 b) -31 and +29 c) -1 and +7 d) +7 and -8 e) +26 and -30
5x2M

4) A) Write Verilog code for 16-bit ripple carry adder constructed using 4-bit ripple carry adders. (10)

B) i) Write Verilog code to convert an n-bit binary number into equivalent grey code. **5M** (10)
ii) Draw the logic diagram of full adder. Write the truth table for full adder and derive the equations for Si and Ci+1. **5M**

5) A) i) Implement three-input XOR function using (10)
a) 2-to-1 MUX **4M**
b) 4-to-1 MUX **3M**
ii) Implement three-input majority function using 2-to-1 MUX **3M**

B) i) Write Verilog code for a 4-to-16 decoder constructed using 2-to-4 decoders. **6M** (10)
ii) A combinational circuit is specified by the following three functions:
F1=X'Y'Z'+XZ F2=XY'Z'+X'Y
F3=X'Y'Z+XY
Design a circuit for F1, F2 and F3 using a decoder and other gates. **4M**

6) A) Design a synchronous counter with the repeated binary sequence 0, 1, 2, 4, 5, 6. Use JK flip flops. (10)

B) Design a sequential circuit which has three flip flops, A, B, C; one input, x; and one output, y. The state diagram is given in Fig Q.6.B. Use D flip flops. (10)

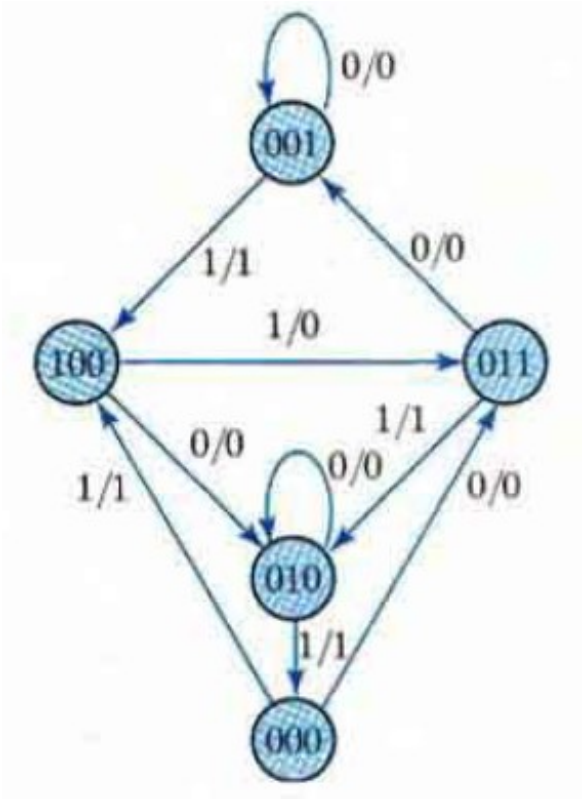

Fig. Q.6.B

7) A) Design a 4-bit bi-directional shift register for the following operations using D flip flops and MUXs. (8)

S_1S_0	Operation
00	No change
01	Right shift
10	Left shift
11	Parallel load

B) Write behavioral verilog code for N-bit shift register. (6)

C) Draw the logic diagram of JK flip flop. Write its characteristic table, characteristic equation and excitation table. (6)

8) A) Explain the following with a neat diagram for each. (12)
i) NMOS realization of a NAND gate. **3M**
ii) NMOS realization of a NOR gate. **3M**
iii) CMOS realization of a NAND gate. **3M**
iv) CMOS realization of a NOR gate. **3M**

B) i) Discuss PLA with a neat logic diagram. **6M** (8)
ii) Define a tri-state buffer. Write its truth table. **2M**

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