Question Paper

Exam Date & Time: 01-Dec-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
IV SEMESTER B.S. ENGG. END SEMESTER EXAMINATION - NOV./ DEC. 2018
Computer Architecture [CS 242]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) Explain cache coherence problem with an example. Give two possible solutions for the same. (10)

B) Write short notes on the following: (10)
i) Time shared common bus
ii) Interprocessor serial arbitration
iii) SIMD
iv) MIMD
(4 + (3 Ã— 2)

2) A) i) Discuss the different types of access methods in computer memory. (10)
ii) Define access time and memory cycle time. (8+02)

B) Discuss the functioning of micro-programmed control unit with a neat sketch. (10)

3) A) Explain the strobe control method of asynchronous data transfer with neat diagrams. (10)

B) i) Explain 32-bit IEEE floating point format. (10)
ii) (a) Represent 2.6875 in 32-bit floating point format.
(b) Interpret 10111101100000000000000000000000 using 32-bit floating point format.
(6+4)

4) A) Write about register direct, memory direct, memory indirect, displacement and register indirect addressing modes. Draw diagram for each. (10)

B) i) Discuss the register organizations of MC68000, 8086 and 80386. (10)
ii) Write the functions of instruction register, program counter and memory address register.
(7 + 3)

5) (8)

A) A 4-way set-associative cache consists of a total of 64 lines (blocks). The main memory has 4096 lines, each consisting of 128 words.

i) How many bits are there in a main memory address?

ii) How many bits are there in each of the TAG, SET and WORD fields?

iii) If the cache is an associative cache, how many bits will be there in each of the TAG and WORD fields?

iv)If the cache is a direct mapped cache, how many bits will be there in each of the TAG, LINE (BLOCK) and WORD fields? (4x2)

B) Discuss the concept of overlapped register windows. (12)

6) i) Discuss the evolution of PowerPC. (10)

A) ii) With a suitable example, explain the use of stack in nested procedure calls.

B) Write the set of instructions using 0-address, 1-address, 2-address and 3-address instructions to evaluate the statement R=(A-B) / (C+D*E) (10)

7) With neat diagram discuss RAID 0, RAID 1, RAID 2, RAID 3 and RAID 4 levels. (10)

A)

B) i) Write about seek time and rotational latency, disk access time. (7)

ii) In a disk system there are 39 recording surfaces. The diameter of each recording surface is 50 cm and the inter-track gap is 0.5 mm. All the disks are double-sided disks except for one disk. There is an average of 360 sectors per track and each sector contains 512 bytes of data.

a) How many disk platters are there in the disk system?

b) What would be the maximum number of tracks in a double-sided disk?

c) How many cylinders shall be there in the entire system?

d) What would be the capacity of the disk system?

C) Define cache memory. Draw the diagram for a typical cache organization (3)

8) Explain Booths algorithm for 2's complement multiplication with a neat flow chart. Multiply 7 and -6 using this algorithm. (10)

A)

B) Discuss DMA controller with a neat block diagram. (10)

-----End-----