Question Paper

Exam Date & Time: 30-Nov-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
IV SEMESTER B.S. ENGG. END SEMESTER EXAMINATION - NOV./ DEC. 2018
VLSI Design [EC 245A]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) Explain the working of enhancement N-MOS transistor in cut-off, linear and saturation regions. Draw voltage current characteristics and explain (10)

B) Derive the required ratio between $Z_{p.u.}$ and $Z_{p.d.}$ if an nMOS inverter with depletion mode pull up is to be driven from another nMOS inverter with depletion mode pull up . (10)

2) A) With the help of neat circuit diagram and curve, explain the working of CMOS inverter. Derive the expression for V_{inv}. Discuss the merits of CMOS inverter over NMOS inverter with depletion load. (10)

B) Calculate the effective capacitance for the given multi-layer structure in Figure 2B for 5µm process. Relative Capacitance value for metal1= 0.075, polysilicon=0.1 and Gate to channel = 1.0. (10)

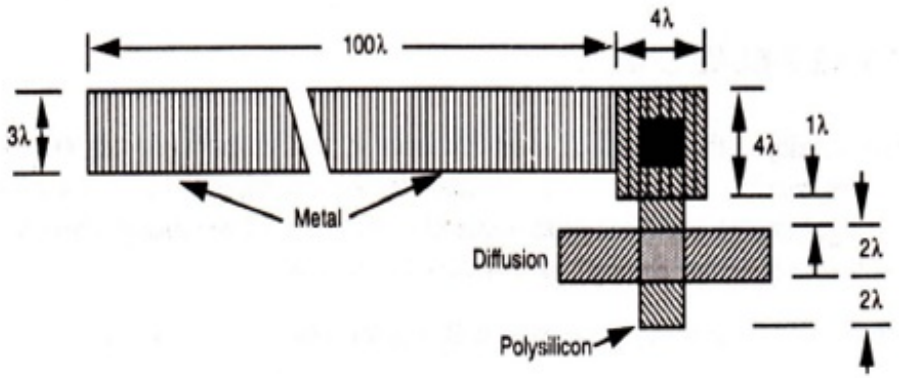

Figure 2B

3) Show that the inverter pair delay using two identical (10)

A) pseudo-NMOS inverters is larger by a factor 1.7 than that using minimum size NMOS inverters with depletion-mode pull-up.

B) Discuss about formal estimation of CMOS Inverter delays and derive the necessary expressions for rise time and fall time. (10)

4) A) Define latch-up in CMOS. Why does it occur? What are the remedies for latch-up? Explain in detail with necessary circuit diagrams and curve. (10)

B) With neat figures explain the different steps involved in the fabrication of CMOS inverter using SOI technique. Write the merits and demerits of SOI technique. (10)

5) A) Discuss the structured design implementation of (n+1)-bit parity indicator block that is provided with bit input word An A_{n-1} A_{n-2}.....A_1A_0.The circuit has one bit parity output P. P will be HIGH (LOW) for even (odd) number of 1s at input. Give the stick notation for CMOS implementation of standard cell. (10)

B) Compare and contrast CMOS and Bipolar technologies. (10)

6) A) Give hardware implementation for storing following 4-bit words using NMOS ROM structure. word1: 0101 ; word2: 0010 ; word3: 1001 ; word4: 0110 (10)

B) Give the circuit implementation of following multiple output function using NMOS based PLA. Give the stick notation. (10)

$$Z_1 = AB + \bar{A}\bar{B}C \; ; \; Z_2 = AB \; ; Z_3 = A + \bar{B}C$$

7) A) Design the circuit of **Figure 7A** so that transistor operates at I_D= 0.4 A and V_D = 0.5V.The NMOS transistor has V_t= 0.7V, μ_nCox = 100 μA/V^2, L= 1μm and W= 32 μm.Neglect the channel length modulation effect. (10)

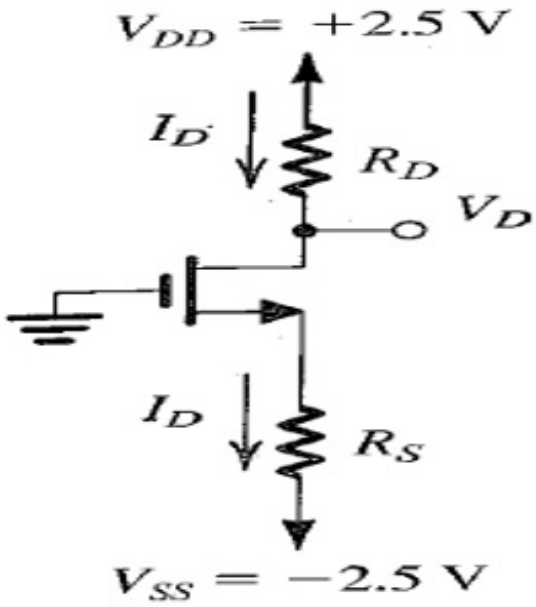

Figure 7A

B) Explain different scaling models. Discuss the effect of all scaling on following parameters: (10)

[i] Gate area A_g

[ii] Gate capacitance per unit area C_o

[iii] Carrier density in channel Q_{on}

[iv] Maximum operating frequency f_o.

8) A) Explain the operation of inverting and non- inverting super buffer. How does super buffer avoid unequal rise and fall delay in NMOS inverters? Give proper justification. (10)

B) Discuss cascaded inverters as drivers for driving large capacitive loads and derive the necessary expressions. (10)

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