Reg. No.											

MANIPAL INSTITUTE OF TECHNOLOGY

(A constituent unit of MAHE, Manipal 576104)

III SEM B. Tech (BME) DEGREE MAKE UP EXAMINATIONS, DEC/JAN 2018-19

SUBJECT: ANALOG ELECTRONICS (BME 2102)
(REVISED CREDIT SYSTEM)
Saturday, 22nd December 2018: 9AM to 12 NOON

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to Candidates:

1. Answer ALL questions.
2. Draw labeled diagram wherever necessary

1A. For the circuit shown in Fig 1A, determine the operating point and also draw the load line. Given $\beta = 100 \& V_{BE} = 0.7V$. 3

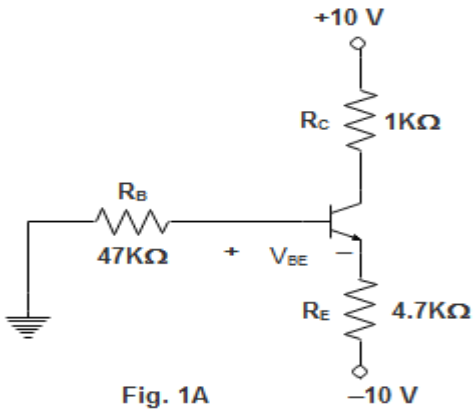

Fig. 1A

1B. How different is fixed-bias circuit from a collector to base bias circuit? Provide reasons with the help of circuits and expression for stability factor. 3

1C. A two stage FET oscillator network uses a phase shifting network shown in Fig Q1C. Determine expressions for its loop gain, frequency of oscillations, minimum gain required for oscillations. 4

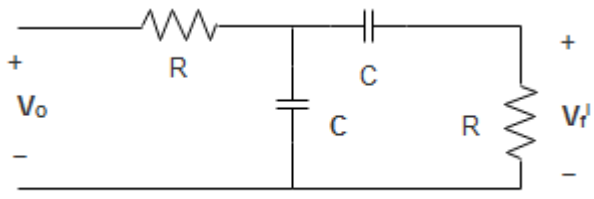

Fig.Q1C

2A. Why RC coupling is effective for frequencies greater than 10 Hz in a multistage amplifier? How RC coupling is different from transformer coupling in the case of multistage amplifiers? Give reasons with the help of circuit. 3

2B. Derive an expression for the frequency of oscillation of a Hartley oscillator. 3

2C. An RC phase shift oscillator has the phase shifting network in its feedback path. Determine the expression for the input impedance of the phase shifting network. 4

3A. Arrive at an expression for the overall low 3 dB frequency of multistage amplifier having non-interacting stages. 3

3B. With the help of circuit explain mathematically the effect of capacitor C_b on the low frequency response of an RC coupled stage. 3

3C. A three stage RC coupled amplifier uses FETs with the following parameters: $g_m = 2.6mA/V$, $r_d = 7.7K$, $R_D = 10K$, $R_g = 0.1M$, $C_b = 0.005\mu F$ and $C_S = 60PF$ for each stage. Evaluate overall mid band voltage gain in decibels, lower 3 dB frequency and overall lower 3 dB frequency. 4

4A. Design a phase shift oscillator to operate at a frequency of 5 KHz. Use MOSFET with $\mu = 55$ and $r_d = 5.5K$. The phase shift network is not to load down the amplifier. 3

a) Find minimum value of the drain circuit resistance R_D for which the oscillator will oscillate.

b) Find RC time constant.

c) Choose a reasonable value for R and find C.

4B. Design a suitable feedback amplifier circuit that is required to provide a gain of 4 and input impedance with feedback 50 KΩ. 3

4C. For a class B power amplifier providing a 20 V peak signal to a 16 ohm load and a power supply of 30 V, determine input power, output power and efficiency. 4

5A. How class A power amplifier is different from Class B power amplifier? Discuss with the help of circuit diagram and suitable waveforms. 3

5B. Arrive at the expression for the maximum efficiency of a class B power amplifier. Use suitable circuit and waveforms for arriving at the solution. 3

5C. Design a suitable audio frequency oscillator circuit that is required to provide oscillations with the help of stability factor 6. 4