Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2018

SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ELE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 24, November 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Given the network of Fig Q1A, determine the functions f_2 and f_3 if f_1 = B and the overall function is to be

$$F(A,B,C,D)=\prod M(1,3,9,11,12,13,14)+d(2,8)$$

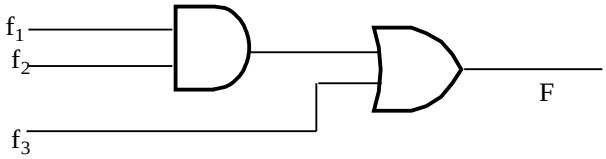

Fig Q1A ***(03)***

1B. Show how $F = A + B + \overline{C}$ can be implemented with one 2 input NAND gate and one 2 input NOR gate. ***(02)***

1C. Obtain a minimal SOP expression using Tabular method for the following equation.

$$F(A,B,C,D)=\sum m(2,4,7,9,11,12,14)+d(0,5,6,13,15)$$ ***(05)***

2A. Design a 2 bit comparator circuit as shown in the Fig Q2A using 1:16 D-mux and residual - gates

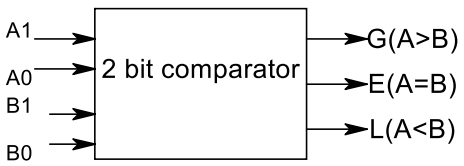

Fig Q2A ***(04)***

2B. Write the truth table and design BCD to Seven-segment decoder circuit using common anode configuration ***(04)***

2C. Implement , 8-bit addition and subtraction operation using IC 74LS283 ***(02)***

3A. Design asynchronous mod-16 up/down counter using positive edge triggered T Flip-flops. Draw the waveform for the same. ***(03)***

3B. Design a one minute counter using decade 7490 IC's ***(03)***

3C. Design two circulating zeros counter using

1. IC 74LS194
2. Implement the same using D flip-flops ***(04)***

4A. A sequential circuit has two inputs, w1 and w2 and an output Z. Its function is to compare the input sequences on the two inputs. If w1= w2 during any four consecutive clock cycles, the circuit produces Z=1 otherwise Z=0. Obtain a suitable Moore state diagram. ***(03)***

4B. Implement the expression $Y = A + B$ using CMOS logic ***(03)***

4C. Draw an ASM chart for the coffee vending machine, as a Moore machine, with the following specifications. The coffee costs Rs.5. The network has 3 inputs F, T, O and two outputs coffee (A) and the change (B). The coin detector inputs a single 1 to the F, T, O for every Rs.5, Rs.2 or Rs.1 respectively. Only one input will be asserted at a time. The coin return mechanism returns changes as multiples of Rs.1. For every 1 output on C, the coin return mechanism returns 1 rupee. The coffee will be dispensed when the network outputs A=1.The network should be reset after dispensing the coffee. Assume that the customer does not insert coins with a total value more than 5. ***(04)***

5A. Design and Implement a synchronous sequential circuit having the following description. The circuit has a mode control input m.

a) if m=1 the sequence of the circuit is 1-3-5-7-1-3…repeats

b) if m=0 , the circuit holds the present state.
Implement the circuit using JK Flip flops.

(06)

5B. Write the state table representation of the FSM with the flip-flop input equations and output decoder equations

$T1=Q_2x$; $T2=X$; $Z=Q_1Q_2$

Where T1 And T2 Are the flip flop inputs, X is the external input Z Is the external output, Q1 and Q2 are the flip flop states. Draw the complete circuit diagram of the FSM. Implement the Next State Decoder and Output decoder using 4 to 1 multiplexers. ***(04)***