Reg. No.									

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent Institution of MAHE, Manipal)

III SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)
MAKE UP EXAMINATIONS, DECEMBER 2018
SUBJECT: DIGITAL ELECTRONIC CIRCUITS [ELE 2102]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 27, December 2018** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. A circuit is to accept two 2 bit binary numbers X_1X_0 and Y_1Y_0 and generate the product as a 4 bit binary number $Z_3Z_2Z_1Z_0$. Implement the circuit using only NAND gates. ***(05)***

1B. Using VEM techniques, simplify the following expression

F(A,B,C,D,E) = ∑m(3.11.14.24.28) + d(0.1.2.4.5.7.15.16.17.20,21,26,29,30,31) where E is the MEV ***(05)***

2A. Implement full subtractor using a) Single dual 4:1 mux

b) 3:8 decoder

c) 2 half subtractor ***(06)***

2B. Design a circuit using 74LS283 that will perform two digit BCD addition, explain the logic used ***(04)***

3A. Design a presettable counter which can count the states 9,10 ,11,12,13,14,15 using

a) T flip-Flop

b) D Flip-Flop ***(04)***

3B. What is Race around condition? Explain, how it can be over come. ***(02)***

3C. Using a 4 bit universal shift register (74LS194) design a sequence generator which cycles through the following sequence 0-8-12-6-13-11-7-3-1-0 ***(04)***

4A. Design and Implement a Moore machine to detect the sequence 1111 using D flip flops. ***(03)***

4B. Implement the expression $Y = \overline{(AB) + (CD)}$ using CMOS logic ***(04)***

4C. Draw an ASM chart for the given state table.

Present state	Input	Next state	Output
T1	00	T2	0
T1	01	T3	0
T1	10	T1	0
T1	11	T3	0

(03)

5A. Design and Implement a synchronous sequential circuit having the following description. The circuit has a mode control input m.

a) if m=0 the sequence of the circuit is 3 bit 0-2-4-6-..repeats
b) if m=1 , the circuit generates 1-3-5-7…..repeats

Implement the circuit using T flip flop. ***(06)***

5B. Draw the state diagram and state table representation of the FSM with the Flip-Flop input equations and output decoder equations

D1=(Q1+Q2)x ; D2=(Q1+ $\overline{Q_2}$.) x ; Z=Q1Q2 x

Where D1 and D2 are the flip flop inputs, x is the external input Z is the external output, Q1 and Q2 are the flip flop states ***(04)***