Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE – 2101)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design the circuit of Figure 1A for a voltage gain of 10 with Q_1 operating at the edge of saturation. Calculate the bias current and the value of R_C if $\beta = 100$, $I_S = 5 \times 10^{-16}$ A, and $V_A = \infty$. Calculate the input impedance of the circuit.

1B. For the circuit in Figure 1B, write an expression for voltage gain and the I/O impedances. Assume $V_A = \infty$.

1C. In the circuit of Fig. Q1(c), I_1 = 1mA, $I_S = 3\times10^{-17}$A. (a) Assuming $V_A = \infty$, determine V_B such that I_C = 1 mA. (b) If V_A = 5V, determine V_B such that I_C = 1 mA for a V_{CE} of 1.5V.

(4+3+3)

2A. Design a common source amplifier for a voltage gain of 5 and input impedance of more than 10kΩ. Restrict the power budget within 5mW. Assume $\mu_n C_{ox}$=100μA/V^2, V_{TH}=0.4V, λ=0 and V_{DD}=1.8V.

2B. Consider a NMOS transistor with W=2μm, L=0.18μm and 0.7V across its gate and source terminals. Determine its all small signal parameters. Assume $\mu_n C_{ox}$ = 100μA/V^2, V_{TH}=0.4V, λ=0 and V_{DD}=1.8V.

2C. Determine the gain and output impedance for the circuit shown in Figure 2C. Assume λ=0.

(4+3+3)

3A. Compute the poles of the circuit shown in Figure 3A assuming λ = 0. If both M_1 and M_2 are identical and R_S = 200 Ω, C_{GS} = 250fF, C_{SB}, C_{GD} = 80fF, C_{DB} = 100fF, $g_m = (150\Omega)^{-1}$, calculate the poles with the aid of Miller's approximation.

3B. Assuming $\lambda > 0$ and using Miller's theorem, determine the input and output poles of the stage depicted in Figure 3B.

3C. Design the source follower depicted in Figure 3C for a voltage gain of 0.8 and a power budget of 2mW. Assume the output dc level is equal to $V_{DD}/2$ and the input impedance exceeds 10 kΩ.

(4+3+3)

4A. Find the closed loop gain, I/O impedance of the circuit shown in Figure 4A. Assume λ=0.

4B. For the circuit shown in Figure 4B, identify the sense, return mechanism and polarity of feedback.

4C. List the salient features of negative feedback amplifier. (4+3+3)

5A. For the circuit shown in Fig. Q5(a), obtain the expressions for gain and frequency of oscillation. Also, extend the result for Hartley and Colpitt's oscillator.

5B. Derive an expression for efficiency of Class A Push - Pull power amplifier.

5C. Determine the region of operation of M_1 as V_1 goes from V_{DD} to zero for the circuit shown in Fig. Q5(c). Assume V_{DD} = 2.5 V and V_{TH} = -0.5 V

(4+3+3)

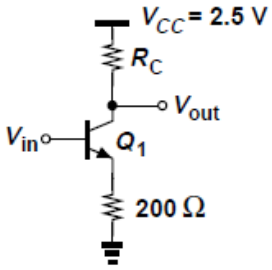

Figure 1A

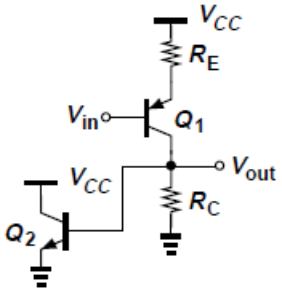

Figure 1B

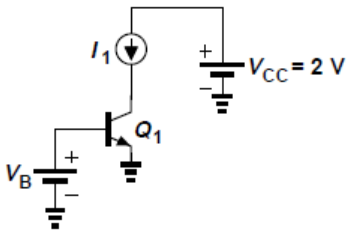

Figure 1C

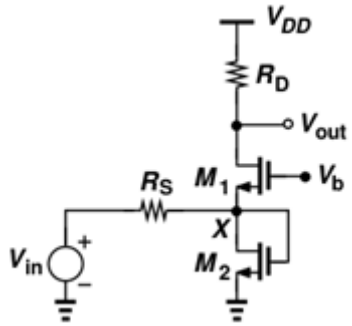

Figure 2C

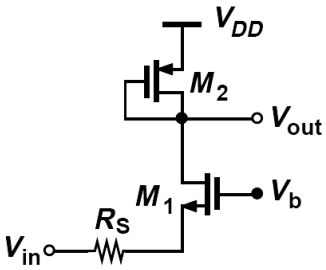

Figure 3A

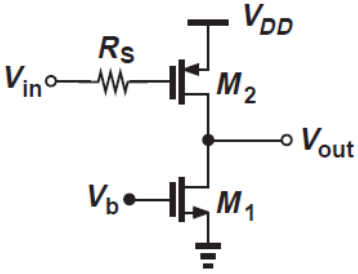

Figure 3B

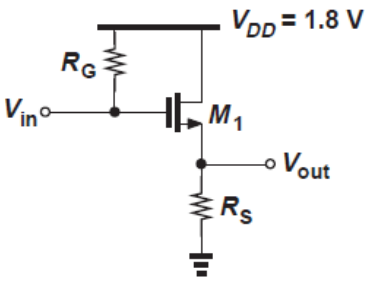

Figure 3C

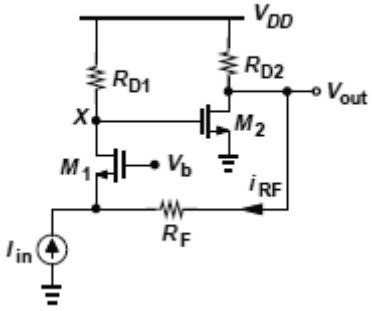

Figure 4A

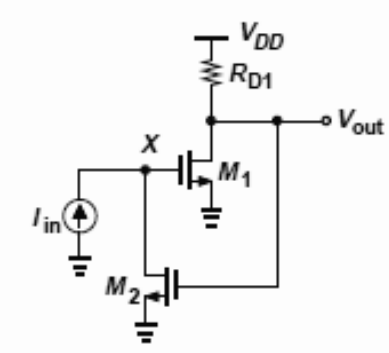

Figure 4B

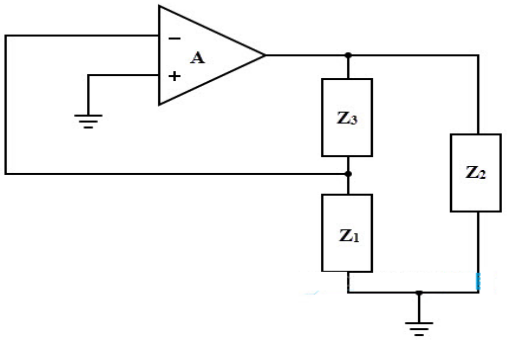

Figure 5A

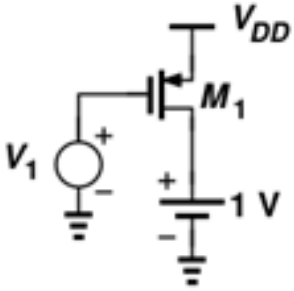

Figure 5C