Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2018
SUBJECT: ANALOG ELECTRONIC CIRCUITS (ECE - ECE 2101)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. The CE amplifier circuit of Figure. Q1(a) must be designed for an input impedance >10kΩ and $g_m = 1/(260\Omega)$. If $\beta = 100$, $I_S = 2\times10^{-17}$A, and $V_A = \infty$, determine the minimum allowable values of R_1 and R_2. Check if the circuit can be redesigned for a $g_m = 1/(26\Omega)$.

1B. For the circuit in Figure. Q1(b), determine the operating point and the small-signal model. Assume $I_S = 8\times10^{-16}$A, $\beta = 100$, and $V_A = \infty$.

1C. For the circuit in Figure. Q1(c), assuming Early effect, write the expression for the voltage gain, input and output impedances.

(4+3+3)

2A. Determine the voltage gain and I/O impedance for the circuit shown in Figure. Q2(a). Assume $\mu_n C_{ox} = 100\mu A/V^2$, $V_{TH}=0.4V$, $\lambda=0$ and $V_{DD} = 1.8V$.

2B. Determine the gain and output impedance for the circuit shown in Figure. Q2(b). Assume $\lambda>0$.

2C. For the circuit shown in Figure. Q2(c) What is the minimum allowable value of V_{DD} if M_1 must not enter the triode region? Assume $\mu_n C_{ox}=100\mu A/V^2$, $V_{TH}=0.4V$, $\lambda=0$ and $V_{DD}=1.8V$.

(4+3+3)

3A. For the CS stage of Figure. Q3(a) Obtain the expressions for poles of the circuit using Miller's approximation. If $R_S = 200\Omega$, $R_D = 1\ k\Omega$, $I_D = 1$ mA, $C_{GS} = 50$fF, $C_{GD} = 10$ fF, $C_{DB} = 15$fF, and $V_{GS}-V_{TH} = 200$mV, using high frequency model of the transistor, calculate the poles.

3B. For the circuit shown in Figure. Q3(b) derive the transfer function of the circuit, substitute $s = j\omega$, and obtain an expression for $|V_{out}/V_{in}|$.

3C. Derive the expressions for low frequency and high frequency poles of CG stage.

(4+3+3)

4A. Find the closed loop gain, I/O impedance of the circuit shown in Figure. Q4(a).

4B. Identify the feedback topology in the block diagram shown in Figure. Q4(b). Find its I/O impedance.

4C. Show that the negative feedback enhances the bandwidth of an amplifier.

(4+3+3)

5A. Explain the working of Ring Oscillator with a neat circuit diagram. Obtain the expressions for gain and frequency of oscillation.

5B. Derive an expression for efficiency of Class B push - pull power amplifier.

5C. Starting from drain current expression derive the small signal model of MOSFET.

(4+3+3)

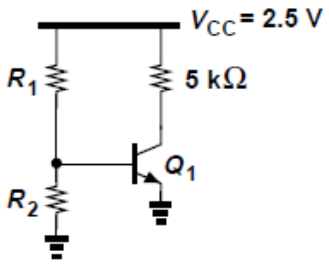

Figure. Q1(a)

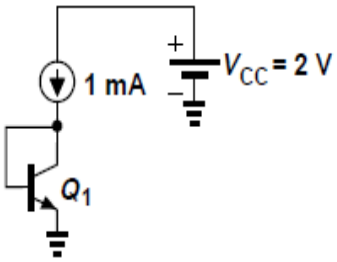

Figure. Q1(b)

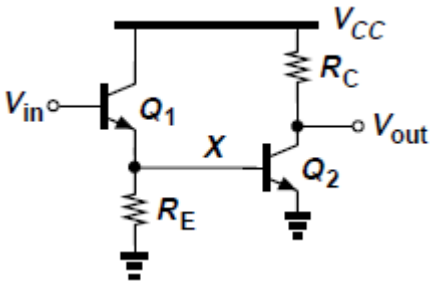

Figure. Q1(c)

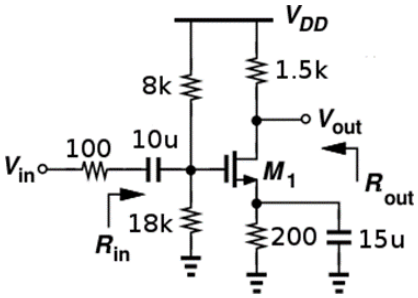

Figure. Q2(a)

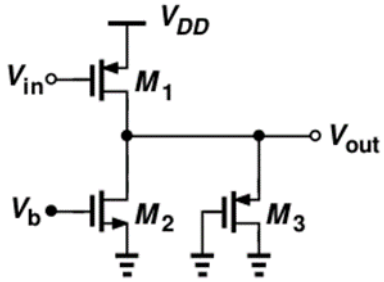

Figure. Q2(b)

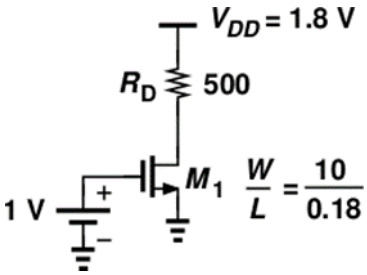

Figure. Q2(c)

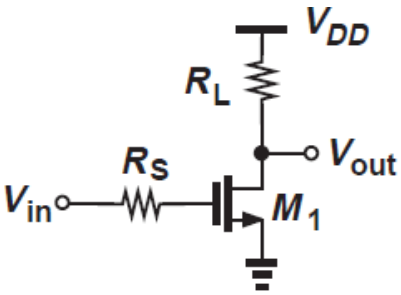

Figure. Q3(a)

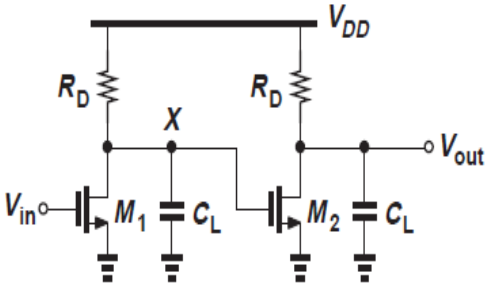

Figure. Q3(b)

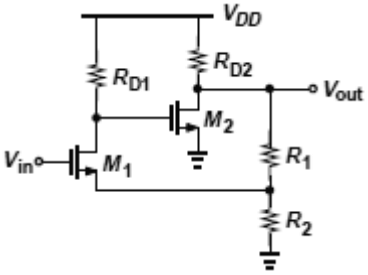

Figure. Q4(a)

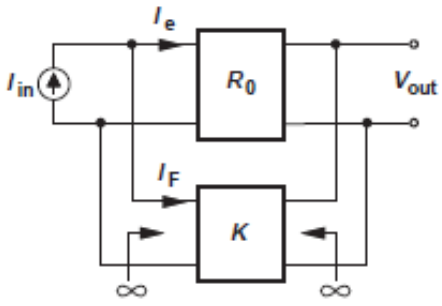

Figure. Q4(b)