Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
NOVEMBER 2018
SUBJECT: LOGIC DESIGN (ECE - 2105)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Using Quine McCluskey method obtain all the prime implicates for f(w,x,y,z)= ΠM(0,2,3,4,5,12,13)+d(8,10)

1B. Design 4 bit binary to gray code converter using only half adders.

1C. Define and explain the following with necessary diagrams:
i. Noise Margin ii. Propagation Delay.

(4+3+3)

2A. Realize the Boolean expression f(w,x,y,z) =∑m(4,5,7,8,10,12,15) using 4:1 MUX and external gates with y and z as the select lines S_1 and S_0 respectively.

2B. Implement $f_1(x,y,z) = \sum m(0,1,3,5)$ and $f_2=\sum m(3,5,7)$ using 3 x 4 x 2 PLA

2C. Implement 2-bit magnitude comparator using 3:8 decoder with active low enable and outputs.

(4+3+3)

3A. Design a self-correcting synchronous counter whose counting sequence is “010”, “111”, “101”, “000”, “001”, “010”……. Use positive edge triggered T flip-flops.

3B. Design a digital circuit which adds two 4-bit binary numbers when control signal is high and subtracts the second number from the first, when control signal is low. Use 4-bit binary adder IC.

3C. Realize a negative edge triggered JK flip-flop using a negative edge triggered SR flip-flop.

(4+3+3)

4A. Design a synchronous sequential circuit which has two inputs and one output. After each clock, it adds the two inputs along with the carry generated in the previous addition and updates the memory with new carry generated. Use Moore model and D flip-flops.

4B. Design a synchronous sequential circuit which divides the frequency of a train of pulses by 6. Use D flip-flops.

4C. Draw ASM chart for 3-bit synchronous up counter.

(4+3+3)

5A. Draw next state table, state table, flow table and flow diagram for the following asynchronous sequential circuit.

$D_1 = \bar{y}Q_1 + \bar{x}Q_1 + \bar{x}yQ_2$ $D_2 = xQ_1 + yQ_1Q_2 + xQ_2 + xy$ $z = \bar{y}Q_1 + \bar{x}Q_1Q_2 + x\bar{y}Q_2$

5B. Design a 3-bit parallel-in serial-out shift register using D flip-flops.

5C. Draw the logic diagram of Master-Slave JK flip-flop and write the truth table.

(4+3+3)