Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

THIRD SEMESTER B.TECH. (E & C) DEGREE END SEMESTER EXAMINATION
DECEMBER 2018/JANUARY 2019
SUBJECT: LOGIC DESIGN (ECE - 2105)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Design a combinational shifter circuit shown in **Figure 1A** and whose function is described in **Table 1A**, using suitable combinational logic blocks.

1B. Find the minimal sum for the function given below

$$f(a,b,c,d) = \sum m(0,1,2,3,4,6,9,12,14) + d(5,7,15)$$

1C. Explain the working of TTL NAND Gate with circuit diagram.

(4+3+3)

2A. Design 3-bit binary multiplier using half adder, full adder and necessary logic gates.

2B. Implement 4 to 16 decoder using two 2 to 4 decoder and AND gates.

2C. Find the minimal sum for the given function using VEM technique. Input d is used as map entered variable.

$$f(a,b,c,d) = \sum m(4,5,6,7,8,10,12)$$

(4+3+3)

3A. Design a synchronous counter which counts in the following sequence 0,2,3,6,5,4,0,… using JK flip-flops. Make the counter self starting.

3B. Explain the operation of 4-bit Johnson counter with a neat circuit diagram using D flip-flop and sequence table.

3C. Explain the working of 4-bit carry look ahead adder with logic diagram.

(4+3+3)

4A. Design a sequential circuit using D flip-flops to detect an overlapping sequence "1011". The circuit should produce an output "1" whenever the sequence 1011 is detected.

4B. A sequential circuit consists of 2 JK Flip-flops. X is the input, A&B are the outputs of the flip-flops. The flip-flop input functions are given by J_A=B, $K_A = \overline{X}B$, $J_B = \overline{X}$, $K_B = A \oplus X$. Write excitation table, next state table, state table and state diagram.

4C. Draw the logic diagram of a gated JK latch using NAND gates only. Write the truth table.

(4+3+3)

5A. Design a fundamental mode asynchronous sequential circuit with two inputs S & R and one output Z. When R=1, Z= compliment of S, when R=0, Z holds its value prior to R becoming zero. Assume initial state as S=R=0 and Z=0. Design the circuit using only NAND gates. Show all the design steps.

5B. Design a circuit to implement function $F_1=\sum m(1,2,3,7)$ $F_2=\sum m(3,5,7)$ using 3X4X2 PLA.

5C. Draw the ASM chart for mod-6 up counter.

(4+3+3)

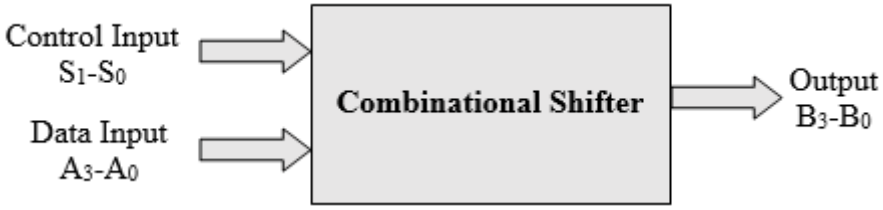

Figure. 1A

Table 1A

S_1S_0	Operation
00	No shift
01	1-bit right shift
10	2-bit right shift
11	3-bit right shift